



Bell Laboratories

NASA-CR-122468

ENERGETIC PARTICLES EXPERIMENT INSTRUMENTATION PACKAGING PROGRAM FOR IMP-F (EXPLORER 34) AND IMP-G (EXPLORER 41) NASA Interplanetary Monitoring Platform Program

W. L. Brown et. al.

Bell Laboratories

Mountain Avenue, Murray Hill, New Jersey 07974

on behalf of

Western Electric Company

83 Maiden Lane, New York, New York 10038

July 1, 1970

Final Report for Contract NAS 5-9102

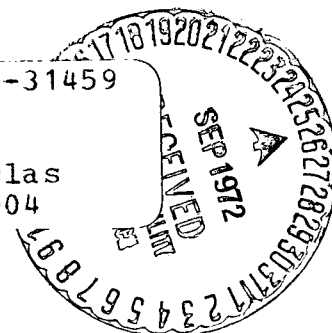
for Period June, 1965—June, 1969

(NASA-CR-122468) ENERGETIC PARTICLES
EXPERIMENT INSTRUMENTATION PACKAGING
PROGRAM FOR IMP-F (EXPLORER 34) AND IMP-G
(EXPLORER 41) NASA (Bell Telephone Labs.,
Inc.) 1 Jul. 1970 98 p

N72-31459

Unclas
41004

CSCL 14B G3/14



Prepared for

GODDARD SPACE FLIGHT CENTER

Greenbelt, Maryland 20771

Reproduced by
**NATIONAL TECHNICAL
INFORMATION SERVICE**
US Department of Commerce
Springfield, VA. 22151

104 PB

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.	
4. Title and Subtitle ENERGETIC PARTICLES EXPERIMENT INSTRUMENTATION PACKAGING PROGRAM FOR IMP-F (EXPLORER 34) AND IMP-G (EXPLORER 41) NASA Interplanetary Monitoring Platform Program		5. Report Date July 1, 1970	
		6. Performing Organization Code	
7. Authors W. L. Brown et. al.		8. Performing Organization Report No.	
9. Performing Organization Name and Address Bell Telephone Laboratories, Incorporated Murray Hill, New Jersey 07974 on behalf of Western Electric Company, Incorporated New York, New York 10038		10. Work Unit No.	
		11. Contract or Grant No. NAS 5-9102	
		13. Type of Report and Period Covered Final Report June, 1965 - June, 1969	
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Goddard Space Flight Center Greenbelt, Maryland 20771		14. Sponsoring Agency Code	
15. Supplementary Notes			
16. Abstract This report describes in detail the package design and assembly techniques for the Bell Telephone Laboratories IMP-F and IMP-G space-physics experiments, provided for the NASA Interplanetary Monitoring Platform Program. Thin-film, hybrid, integrated circuits used in these instruments to increase component density and reliability, and special procedures and precautions for the fabrication of space hardware are described.			
17. Key Words Radiation Measuring Instruments Spaceborne Detectors Extraterrestrial Radiation IMP Space Physics Experiments		18. Distribution Statement	
19. Security Classif. (of this report) U	20. Security Classif. (of this page) U	21. No. of Pages 97	22. Price \$7.00

PRECEDING PAGE BLANK NOT FILMED

PREFACE

This final hardware report describes the particle-detection equipment flown on the IMP-F (Explorer 34) and the IMP-G (Explorer 41) spacecraft. Another final report under this program has summarized the results of reducing and analyzing the particle data acquired from the particle-detection equipment on the two spacecraft. Equipment on IMP-F successfully acquired data from the time of its launch (May, 1967) until destruction upon reentry (May, 1969). The equipment on IMP-G performed perfectly from launch (June, 1969) until a failure in a spacecraft power supply disabled the high-energy-particle identifier modes (February, 1970). After this, the IMP-G equipment has continued to operate successfully in acquiring low-energy proton, alpha particle, and electron data in interplanetary space and in the magnetosphere.

The design, development, fabrication, and testing of the particle-detection equipment described herein represents the coordinated efforts of a number of Bell Laboratories technical personnel including W. L. Brown, G. L. Miller, I. Hayashi, H. P. Lie, L. J. Lanzerotti, L. V. Medford, H. E. Kern, R. W. Kerr, D. A. H. Robinson, J. W. Rodgers, and G. H. Wheatley.

TABLE OF CONTENTS

<u>Paragraph</u>		<u>Page</u>
SECTION 1 — INTRODUCTION		
1.1	Experiment	1
1.2	Package Design	6
SECTION 2 — ELECTRONIC PACKAGING		
2.1	System Design	13
2.2	Integrated Circuits	13
2.3	Printed Circuit Motherboards	16
2.3.1	General Description	16
2.3.2	Motherboard Layout	17
2.4	Electronic Stack Design	47
2.4.1	Physical Description	47
2.4.2	Encapsulation Technique	49
2.5	Detector Mount Design	49
2.6	Housing	53
SECTION 3 — COMPONENTS		
3.1	Reliability and Screening	61
3.2	Thin-Film Integrated Circuits	68
SECTION 4 — CONSTRUCTION		
4.1	Printed Circuit Boards	71
4.1.1	Art Work	71
4.1.2	Fabrication	71
4.1.3	Preparation for Assembly	72
4.2	Assembly Area	72
4.3	Motherboard Assembly	74
4.3.1	Parts Kits and Records	74
4.3.2	Assembly Practices	74

TABLE OF CONTENTS (Continued)

<u>Paragraph</u>		<u>Page</u>
4.3.3	Soldering	77
4.3.4	Testing and Trimming	78
4.3.5	Inspection	79
4.4	Encapsulation	83
4.4.1	Integrated Circuit Encapsulation	83
4.4.2	Motherboard Encapsulation	84
4.4.3	Foam Planing	85
4.4.4	Special Operations	85
4.5	Electronic Stack Assembly	86
4.5.1	Preparations	86
4.5.2	Harness Wiring Procedure	87
4.5.3	Detector Mount Integration	89
4.6	Final Assembly	89
4.7	Delivery	91
	SECTION 5 — HISTORY	93
	References	97

LIST OF ILLUSTRATIONS

<u>Figure</u>		<u>Page</u>
SECTION 1 — INTRODUCTION		
1	IMP-F and -G Detector Telescope and Electronics, Block Diagram	3
2	Cross-Section View of IMP-F and -G Detector Telescope	5
3	BTL Experiment Package for IMP-F and -G	7
4	Electronic Stack for BTL IMP-F and -G Experiments	8
5	BTL IMP-F and -G Experiment Assembly	9
SECTION 2 — ELECTRONIC PACKAGING		
6	Thin-Film Integrated Circuits Used in BTL Experiment System	14
7	Top and Bottom Views of Thin-Film Operational Amplifier	15
8	Design of Ground-Plane Finger Contacts	17
9	Motherboard 1, Component Assembly	20
10	Motherboard 1, Schematic Diagram	21
11	Motherboard 2, Component Assembly	23
12	Motherboard 2, Schematic Diagram	25
13	Motherboard 3, Component Assembly	27
14	Motherboard 3, Schematic Diagram	29
15	Motherboard 4, Component Assembly	31
16	Motherboard 4, Schematic Diagram	33
17	Motherboard 5, Component Assembly	35
18	Motherboard 5, Schematic Diagram	37
19	Motherboard 6, Component Assembly	39
20	Motherboard 6, Printed Circuit	40
21	Motherboard 6, Schematic Diagram (Sheet 1 of 3)	41
21	Motherboard 6, Schematic Diagram (Sheet 2 of 3)	43
21	Motherboard 6, Schematic Diagram (Sheet 3 of 3)	45
22	Motherboard Dimensions	47
23	Motherboard Stack Bracket	48
24	Castellated Nut for Circuit-Board Clamping	48
25	IMP-F and -G Detector Mount	51
26	Detector-Mount Back Plate	53

LIST OF ILLUSTRATIONS (Continued)

<u>Figure</u>		<u>Page</u>
27	Housing Assembly	55
28	Top Cover Assembly	57
29	Bottom Cover Assembly	59

SECTION 4 — CONSTRUCTION

30	IMP-F and -G Experiment, Flight-Hardware Assembly Room	73
31	Parts Kit and Completed Board for Motherboard 6	75
32	Assembly of Motherboard 6	76
33	Foaming Molds for Integrated Circuits	83
34	Electronic Stack Harness Wiring	88
35	Encapsulated Harness	91

LIST OF TABLES

<u>Table</u>		<u>Page</u>
1	Operational Modes, BTL Experiment for IMP-F and -G	2
2	Components Used in BTL IMP-F and -G Experiment	62
3	Specifications and Screening Programs	63
4	Inspection Procedures and Sequence	80

SECTION 1

INTRODUCTION

The increasing number of energetic-particle-producing solar flares during the current period of solar maximum (1968-70) provide more frequent opportunities for the study of solar-flare particles, their spectral distributions and isotopic abundances, and their interplanetary propagation. Bell Telephone Laboratories conceived and instrumented an experiment for two Interplanetary Monitoring Platform (IMP-F and -G) spacecraft to provide fast (few-minutes or less) time resolution during a solar-flare event for the determination of the energy spectra of low-energy electrons, protons, and alpha particles, as well as to obtain information on the possible presence of deuterons, tritons, and He^3 . In order to avoid telemetering each event for subsequent analysis on the ground, an on-board particle identifier^{1*} was used as a key element in the design. In addition to providing fast time resolution, the identifier also provides a means of improving the statistics for the detection of rare particle types.

1.1 Experiment

The identification of particle types and the measurement of the particle energy spectrum are performed in the IMP-F and -G experiment using a four-element, solid-state detector telescope and associated electronics, as shown in Figure 1. The detector telescope is axially symmetric with the symmetry axis perpendicular to the spin axis of the satellite. A cross-section view of the detector telescope is shown in Figure 2. The first two detectors (active areas of 0.43 and 0.96 cm^2 , respectively) are totally depleted, n-on-p, diffused silicon diodes. The last two detectors in IMP-F are lithium-drifted silicon detectors (active areas of 0.96 cm^2 each), vacuum-encapsulated in a windowless package. Sets of lithium detectors similarly encapsulated were flown on the ATS-1 and ATS-2 satellites.³ The last two detectors in IMP-G are lithium-drifted silicon detectors fabricated by Kevex, Inc.

The detector stack is preceded by a defining collimator of 20-degree half-angle, which gives an effective geometrical solid angle of 0.37 steradian. Titanium and nickel foils in front of the first detector serve as light shields and primarily determine the lower limits on the heavy particle energies that can be observed. The detector stack and collimator are housed in an aluminum shielding block that stops high-energy particles incident from the rear or sides of the telescope.

*References are listed on page 97.

Proton and alpha particles up to an energy of approximately 4 MeV/nucleon are distinguished by the amount of energy deposited in stopping in the first two detectors of the telescope. Above this energy, particle species other than electrons are distinguished by the use of a pulse multiplier as a particle-species identifier. Electrons are identified in the lithium detectors by their lack of sufficient energy loss to produce a logic pulse in the thin detector electronics (see Table 1).

TABLE 1. OPERATIONAL MODES, BTL EXPERIMENTS FOR IMP-F AND -G

Mode	Coincidence Condition	Identified Particle	Approximate Energy Range (MeV)	5-Channel Energy Spectrum	Remarks
A	1 $\bar{2}$ - -	Heavily ionizing	$0.6 < p < 1.9$ $1.7 < \alpha < 9.0$	1	
B	1 2 $\bar{3}$ -	Heavily ionizing	$1.9 < p < 4.0$ $9.0 < \alpha < 12$	1+2	
C	1 2 3 $\bar{4}$			1x(1+2+3)	Multiplier check-Modes D,E,F,G,P
D	1 2 3 $\bar{4}$	p	$4.0 < p < 18.0$	1+2+3	
E	1 2 3 $\bar{4}$	d	$5.0 < d < 20$	1+2+3	
F	1 2 3 $\bar{4}$	t	$5.5 < t < 25$	1+2+3	Particle identifying modes
G	1 2 3 $\bar{4}$	He ³	$11 < \text{He}^3 < 72$	1+2+3	
P	1 2 3 $\bar{4}$	α	$16 < \alpha < 80$	1+2+3	
H	- $\bar{2}$ 3 $\bar{4}$	e	$.3 < e < 3$	3	
I	- - 3 4	Lightly ionizing	$2 < e$ $18 < p$	3	
J	- - - -				Singles check
K	- 2 $\bar{3}$ -	Heavily ionizing	$2.2 < p < 4.0$ $8.8 < \alpha < 12$	2	
L	- 2 3 $\bar{4}$			2x(2+3)	Multiplier check-Modes M,N,O
M	- 2 3 $\bar{4}$	p	$4.0 < p < 18$		
N	- 2 3 $\bar{4}$	d	$5.0 < d < 20$		Particle identifying modes
O	- 2 3 $\bar{4}$	t	$5.5 < t < 25$		

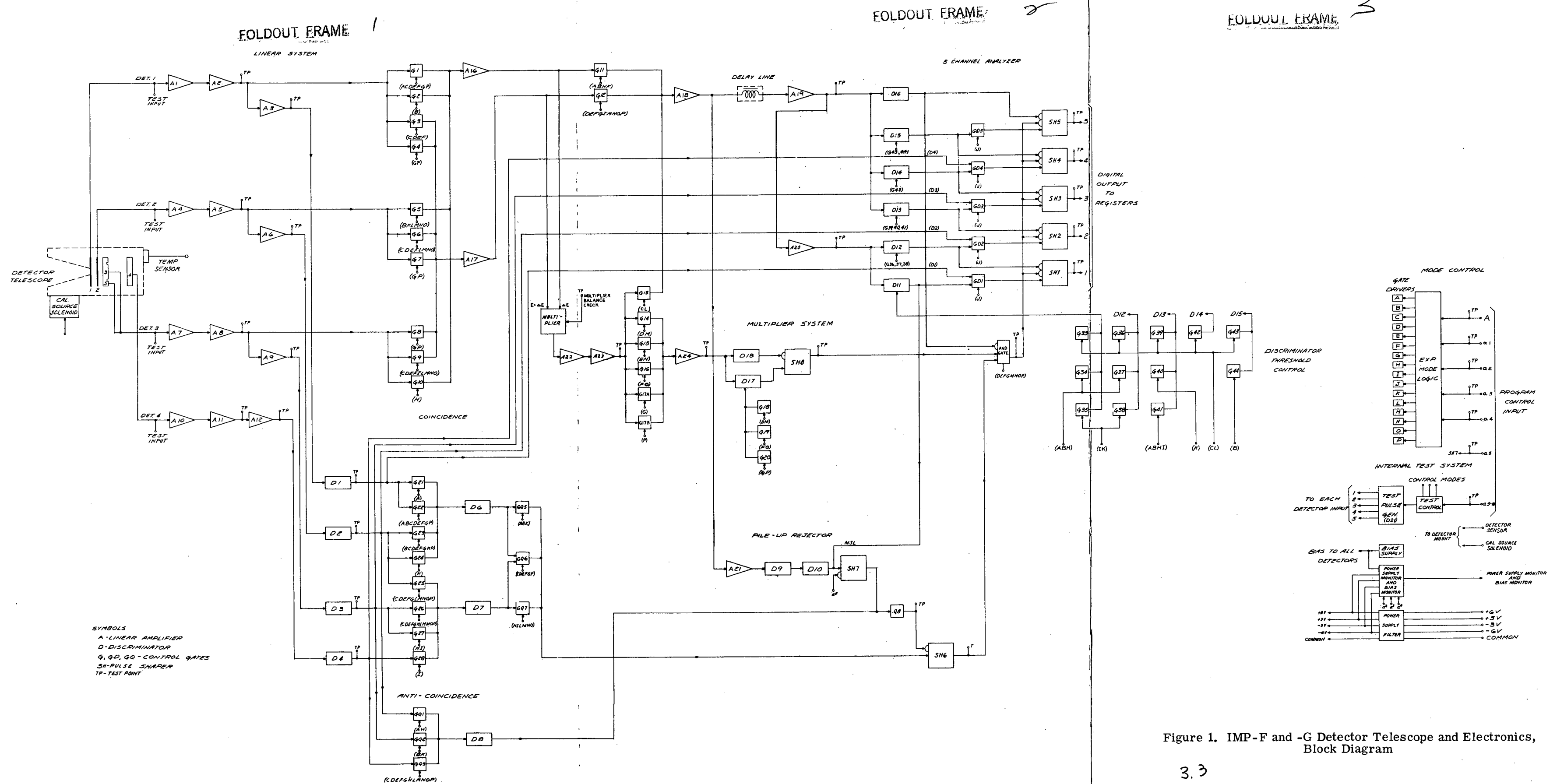
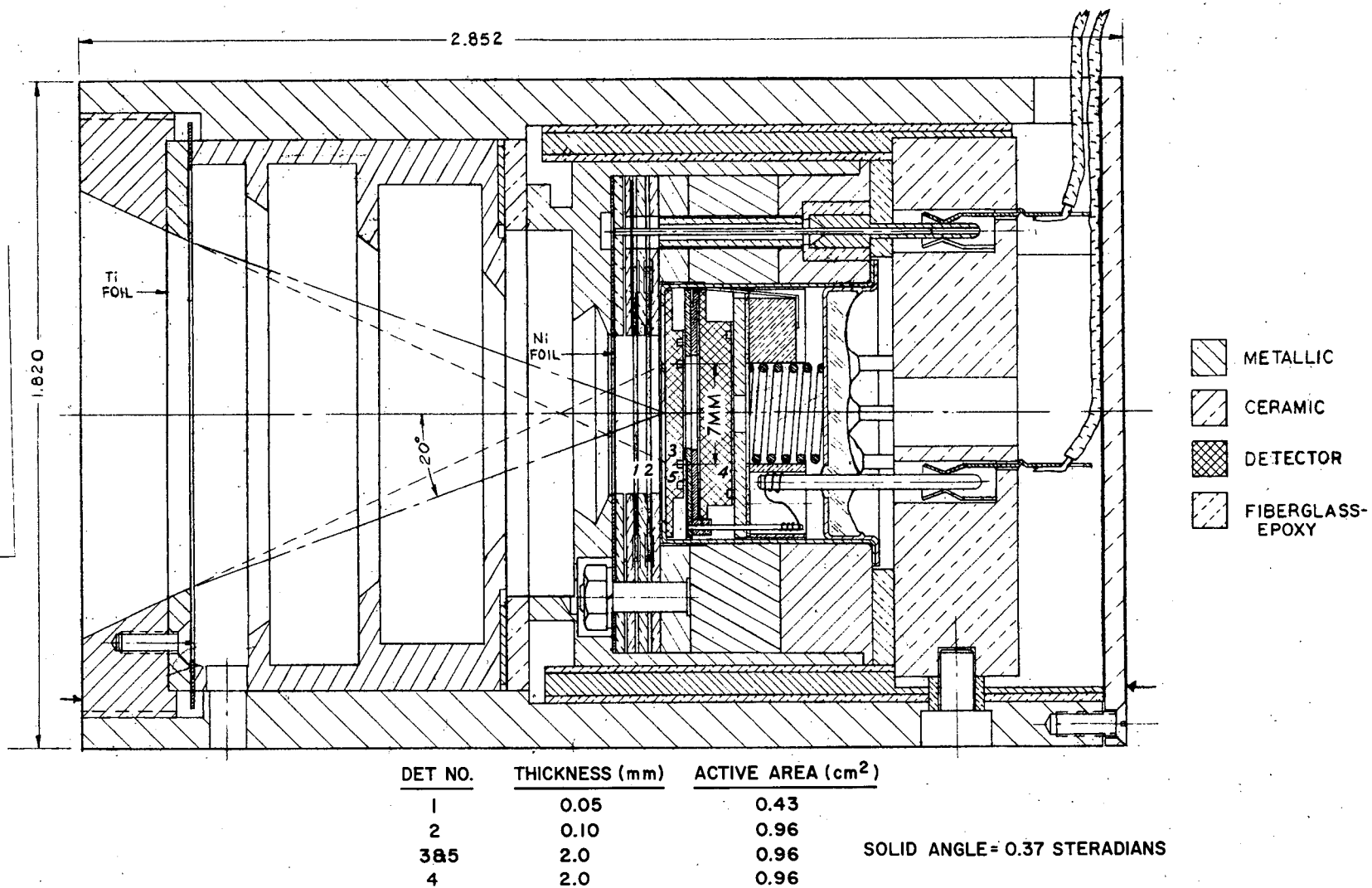


Figure 1. IMP-F and -G Detector Telescope and Electronics, Block Diagram

Preceding page blank



Preceding page blank NOT FILMED

Figure 2. Cross-Section View of IMP-F and -G Detector Telescope

Since the experiment was designed to measure the energy spectra of six different particle species, telemetry limitations required that the experiment operate in a number of sequential modes. During each satellite telemetry sequence (10.227 seconds), a particular set of coincidence, pulse-height, and multiplier-discrimination requirements is established for the pulses from the various detectors. This set of requirements is met by the opening or closing of linear gates, each of which is actuated by a logic circuit driven from the spacecraft sequence clock. Each time a particle event satisfying these conditions occurs during a 9.28-second counting interval within the sequence period, the pulse heights from the detectors in coincidence are summed and analyzed in a five-channel pulse-height analyzer. The digital data from the analyzer, accumulated in five storage registers in the spacecraft digital data processor, are read out at the end of each counting interval. A list of the 16 modes of the experiment and their characteristics are shown in Table 1.

The complexity and precision required of the experiment makes extensive in-flight checks mandatory. During a special calibration sequence, occurring every 6 hours, the detectors are exposed to natural radioactive sources of alphas and electrons. Following this, a ramp pulser connected to all detector preamplifiers causes counting in all modes sufficient to detect electronic drifts on the order of 1 percent.

The power required by the experiment, approximately 1 watt, is supplied by an external supply which furnishes four separate voltage levels. The 200-volt detector bias voltage is internally generated.

1.2 Package Design

The Bell Telephone Laboratories Energetic Particles Experiment is assembled in a 145-cubic inch module 3.6 inches high, weighing 3.9 pounds. A second, smaller module containing the BTL converter and regulated power supply has been furnished by NASA.

Figure 3 is a photograph of a BTL-experiment flight model for IMP-F and -G. The detector telescope aperture is in the lower left corner of the front of the experiment, covered by a thin titanium-foil window. When the large threaded ring which supports the window is unscrewed, the plug-in detector cartridge⁴ and its associated hardware can be removed through the front of the housing. Five coaxial jacks, used for injecting electrical calibration pulses into the experiment, are located to the right of the detector aperture. A miniature, 37-pin connector, near the top edge of



Figure 3. BTL Experiment Package for IMP-F and -G

the front panel, provided access to many test points within the electronic system. The experiment/spacecraft interface connector is located on the back of the housing.

Figure 4 shows the experiment with its housing removed. The internal electronic package consists of a stack of six trapezoidal printed-circuit boards, each individually encapsulated in polyurethane foam for vibration damping and held together by a system of brackets, bolts, and spacers. A horizontal circuit-board configuration was chosen as the most efficient way to utilize the available volume in the rather inconveniently shaped housing. Interconnections between boards are made by wires connected only along their rear edges, to facilitate access to the electronics after final assembly by "fanning" the stack apart from the front.

Figure 5 shows the experiment assembly drawing. Each board is separated from its neighbors by tubular aluminum spacers concentric with long bolts which

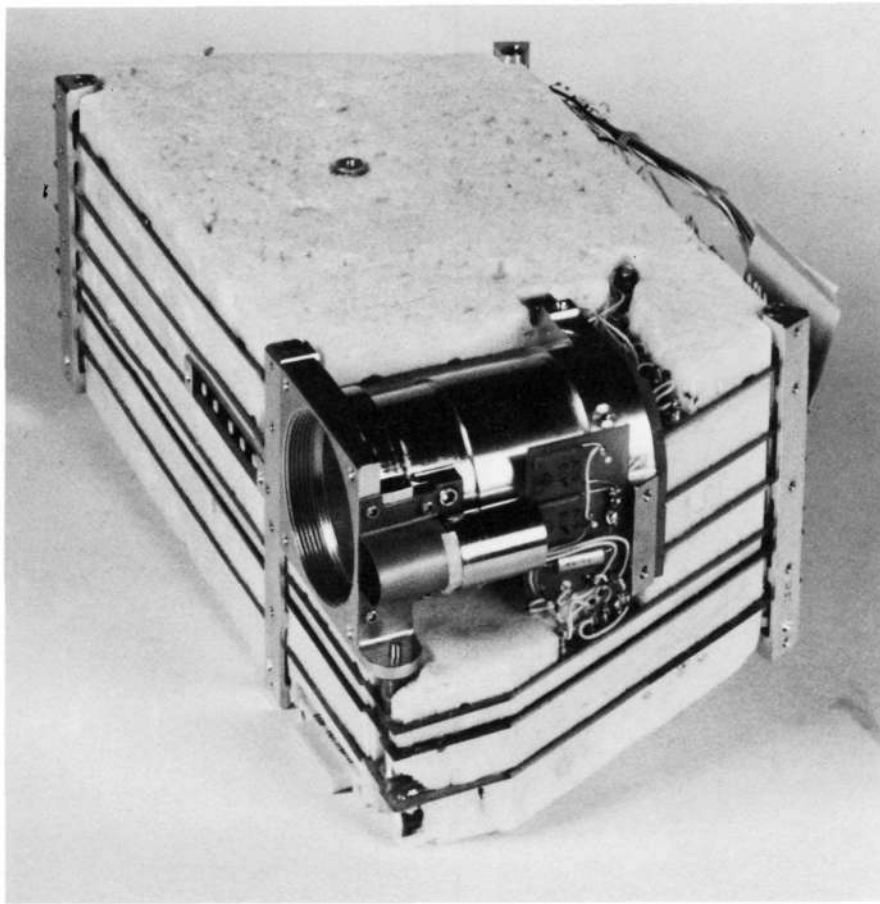


Figure 4. Electronic Stack for BTL IMP-F and -G Experiments

pass through the whole stack in six different places. The ends of four of these bolts are anchored in elongated brackets at the edges of the stack. Tightening special nuts on the threaded ends of the through-bolts brings all boards and spacers under compression and produces a rigid, self-supporting subassembly.

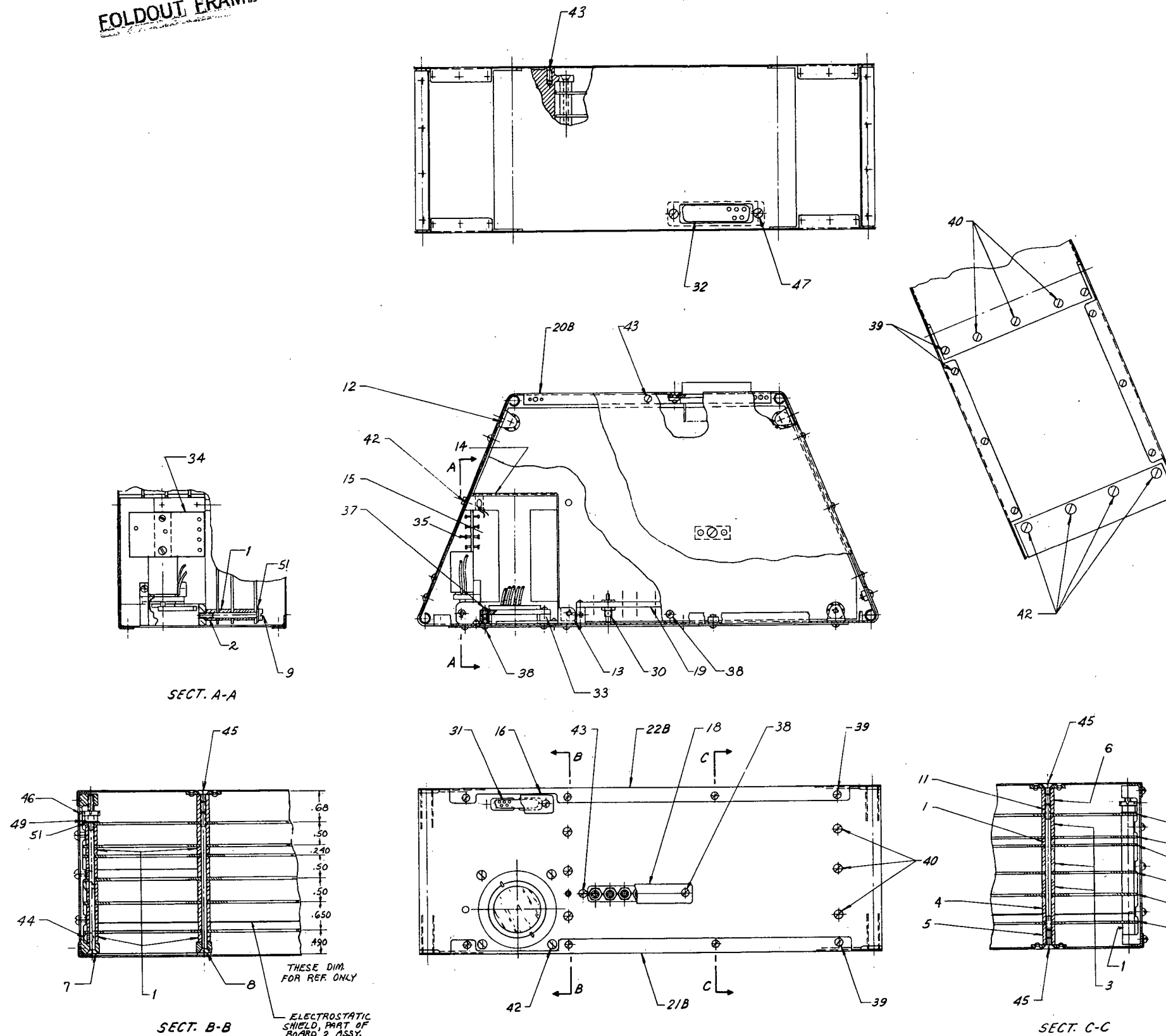
The detector mount is integrated with the stack in one corner, as shown in Figure 5. This location was chosen so that the mount could be secured to both the front plate and left side of the housing, an important consideration for this heavy component to withstand vibrational stress. The appendage shown on the right side of the mount in Figure 4 is an in-flight calibration mechanism⁴ consisting of a semaphore-type arm containing two radioactive sources. The arm is swung into view of the detector by a rotary solenoid at programmed intervals.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

NOTES:

1. MAY BE PURCHASED FROM SELECTRO CORP,
MAMORONECK, N.Y.



5	#4 FLAT WASHER	52
4	B-653176 NUT, CASTELLATED	51
2	SCREW F.H.M. .060-.80 x .187 LG. (100° FH)	50
4	NON-MAG. STN. STL. .112-.40 x .250 LG.	49
3	NON-MAG. STN. STL. .089-.48 x .187 LG.	48
2	NON-MAG. STN. STL. .086-.56 x .187 LG.	47
9	PAN HEAD .112-.40 x .187 LG.	46
14	SCREW, R.H.M. .089-.48 x .150 LG.	45
12	NON-MAG. STN. STL. .086-.56 x .125 LG.	44
24	NON-MAG. STN. STL. .086-.56 x .187 LG.	43
6	NON-MAG. STN. STL. .086-.56 x .187 LG.	42
2	NON-MAG. STN. STL. .086-.56 x .187 LG.	41
6	TERMINAL STUDS	40
1	B-653175 TERMINAL BOARD, DET. MNT.	39
1	B-616085 CONNECTOR BRACKET	38
1	PLUG, CANNON #DBM-25P	37
1	PLUG, CANNON #DBM-37PH13NMC	36
1	RECEPTACLE 50D-043-0000	35
1	B-616525-2 MOTHERBOARD #2	34
1	B-616524-2 " " #5	33
1	B-616523-2 " " #4	32
1	B-616522-1 " " #3	31
1	B-616521-2 " " #2	30
1	B-616520-2 " " #1	29
1	B-615722 TOP COVER ASSEM	28
1	B-615723 BOTTOM COVER ASSEM	27
1	B-615721 HOUSING ASSEMBLY	26
1	B-615780 COAX JACK MOUNT	25
1	B-615779 PLATE	24
1	B-615778 PLATE	23
1	B-615214-1 DETECTOR MOUNT ASSY	22
1	B-616228-1 DETECTOR MOUNT BACK PLATE	21
1	B-615601 BRACKET, CKT. BD. DET.	20
3	B-615600 BRACKET, CKT. BD. STACK	19
1	B-615699 CIRCUIT BOARD STUD	18
1	B-653174 THROUGH BOLT	17
1	B-615597-2 CIRCUIT BOARD BOLT	16
4	B-615597-1 " " " "	15
2	B-615596-2 THREADED SPACER	14
1	B-615596-1 " " " "	13
6	B-615595-4 " " " "	12
10	B-615595-3 " " " "	11
1	B-615595-2 " " " "	10
12	B-615595-1 " " " "	9
29	BOARD-6	8
28	BOARD-5	7
27	BOARD-4	6
26	BOARD-3	5
25	BOARD-2	4
24	BOARD-1	3
23	BOARD-1	2
22	BOARD-1	1

Figure 5. BTL IMP-F and -G Experiment Assembly

The housing-frame members are attached to the electronic stack by screws at the four elongated stack-clamping brackets. Thin top and bottom covers provide electrostatic shielding but do not add structural support.

Three experiment packages were built for the IMP-F program. The first of these was a nonflight, BTL-owned, development model constructed to verify electrical and mechanical designs. This unit was identical to the flight models except that unscreened electronic components were used (though they were the same make and type as those qualified for use in the flight models), and the package was not encapsulated. The construction of a development model has always been worthwhile, not only to investigate design problems and spacecraft interface difficulties but also for continued testing and calibration of detectors after the flight models have been delivered.

Of the two flight models constructed, one was a "proto-flight" which was qualified to environmental test levels exceeding those normally expected in space flight. This model was intended to demonstrate the ability of the system to perform without degradation under possible extreme conditions during spacecraft testing, launch, and orbit. The second model was a flight spare which was tested to environmental exposures equal to those expected during the spacecraft life cycle.

A single flight model was constructed for the IMP-G program. This model was similar to the IMP-F flight model except that the multiplier circuitry was changed slightly to straighten the multiplier response curves in modes M, N, and O.¹ In addition, new low-noise preamplifiers were developed and used. The IMP-F flight spare was used as the IMP-G spare.

Preceding page blank

SECTION 2

ELECTRONIC PACKAGING

The IMP-F and -G programs at Bell Laboratories are concurrent with another for the Applications Technology Satellites (ATS).⁵ The particle experiments for the two projects are similar. Although the geometry is considerably different, the same packaging approach and construction techniques are employed.

2.1 System Design

The IMP-F and -G experiments each contain a total of 2414 electronic components. The complexity of the system, constraints on volume, weight, and power, and the short program schedule led to an approach which would cut design and construction time while retaining high reliability. A hybrid system was chosen, comprising a set of integrated circuit building blocks interconnected and supplemented by additional circuitry using discrete miniature components mounted on printed-circuit motherboards. The block diagram of the system, Figure 1, shows how this was implemented.

2.2 Integrated Circuits

The experiment system contains a total of 91 hybrid integrated circuits,⁶ with resistors made by the tantalum thin-film process on ceramic substrates and all other components appliued. Four basic types of circuits were utilized. These are shown in Figure 6, where (A) is an operational amplifier, shown in detail in Figure 7; (B) is a zero-crossing discriminator, (C) a pulse shaper, and (E) a linear gate. The latter circuit was also designed to adjust gain at various points within the system by suitable parallel combinations of binary weighted resistors interconnected by hand wiring between multiple lands on its substrate. The circuit shown in (D) is a potentiometer network used to replace mechanically adjustable trimming elements in flight hardware. It was produced by the thin-film technique but had no additional components mounted on its substrate.

The thin-film hybrid approach provides

- (a) the best choice of discrete active components from the many commercially available semiconductor devices;

Preceding page blank

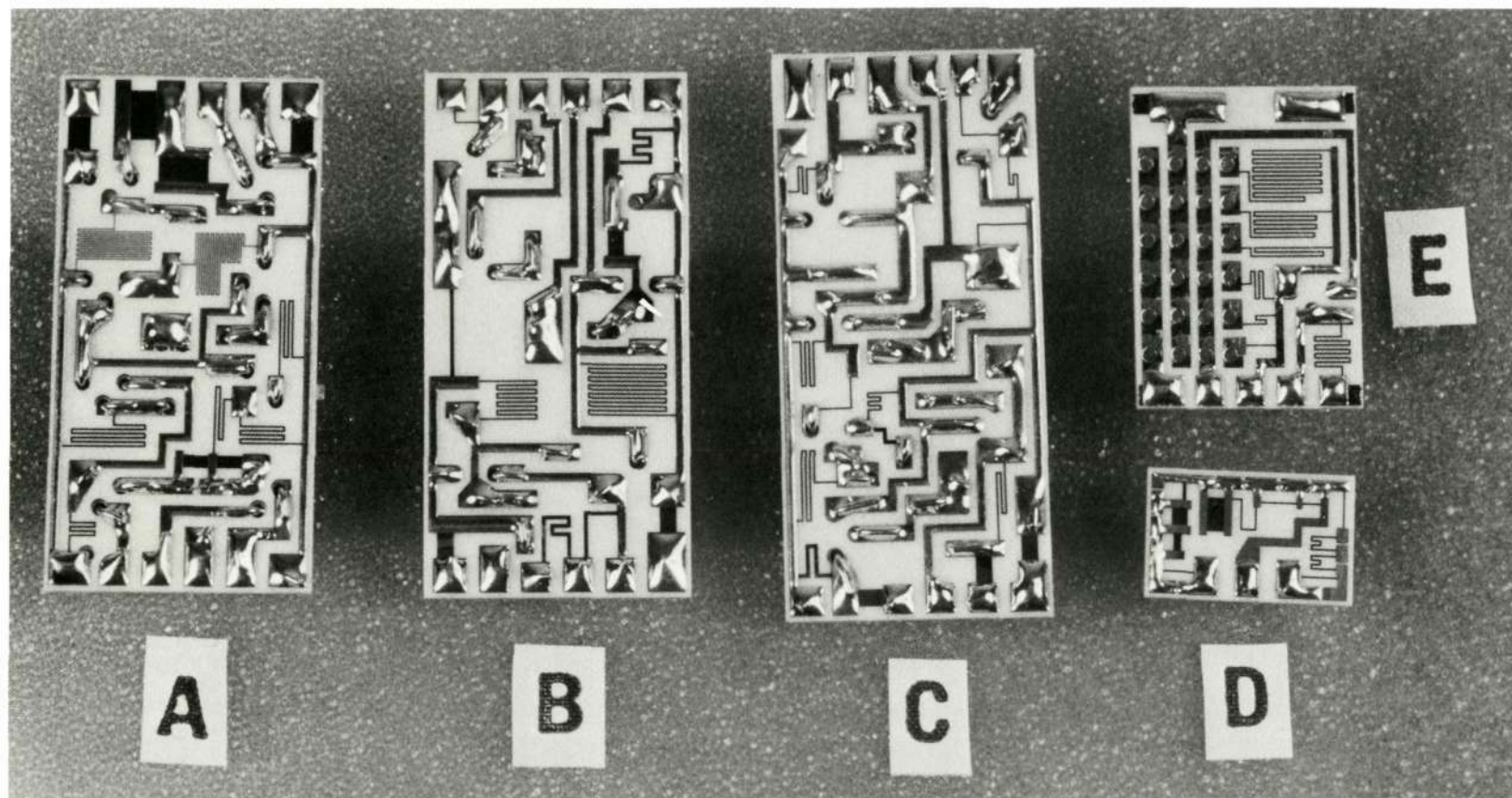


Figure 6. Thin-Film Integrated Circuits Used in BTL Experiment System

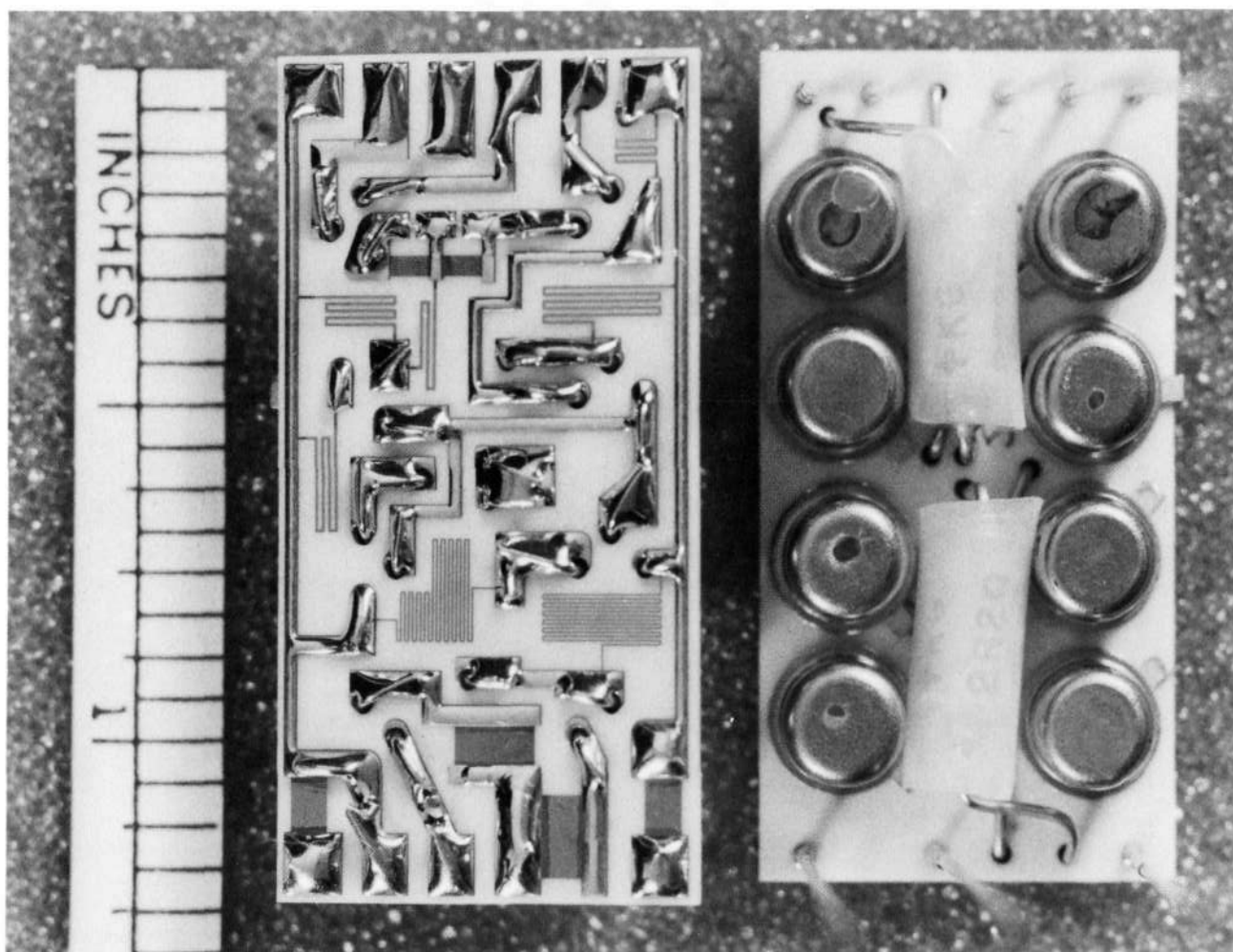


Figure 7. Top and Bottom Views of Thin-Film Operational Amplifier

- (b) essentially unlimited range of resistor values with low temperature coefficient and drift;
- (c) low power through optimum choice of component values and close tolerances;
- (d) no circuit performance problems when going from breadboard to integrated circuit;
- (e) flexibility for design changes if required;
- (f) component density higher than that achievable with cordwood-type packaging: the flat modules can be mounted conveniently on printed-circuit motherboards.

2.3 Printed-Circuit Motherboards

2.3.1 General Description — The electronic systems for IMP-F and -G are each assembled on six printed-circuit motherboards. In most cases, the printed circuit is contained entirely on one side of the board. As much copper as possible was left on the opposite side to serve as a ground plane. The ground plane was extended over the front and side edges of the boards by an electroplating process. With the completed electronic stack assembled in its housing, the plated edges of all boards are interconnected by beryllium copper finger contact sheets mounted inside the front and side members of the housing. The design of the finger contacts is shown in Figure 8. These sheets are electrically insulated from the housing to prevent circulating ground-system dc currents which could disturb spacecraft attitude control and spin rate. Large capacitors provide ac coupling between the signal-ground system and chassis ground at the detector mount. In addition to the obvious electrical advantages of this type of ground system, it also provides a measure of built-in shielding which reduces cross-coupling of signals between motherboards.

All components are mounted on the ground-plane side of each board, which is insulated with a bonded Mylar sheet to protect against short circuits between the copper surface and component leads by accidental inclusion of wire clippings or solder fragments.

Permanent interconnection between motherboards is made by harness wiring soldered to printed terminal lands along the rear edges (visible in Figure 20). These lands were designed to mate with commercial printed-circuit board connectors on a system test stand, a feature which saved considerable time during testing and trimming.

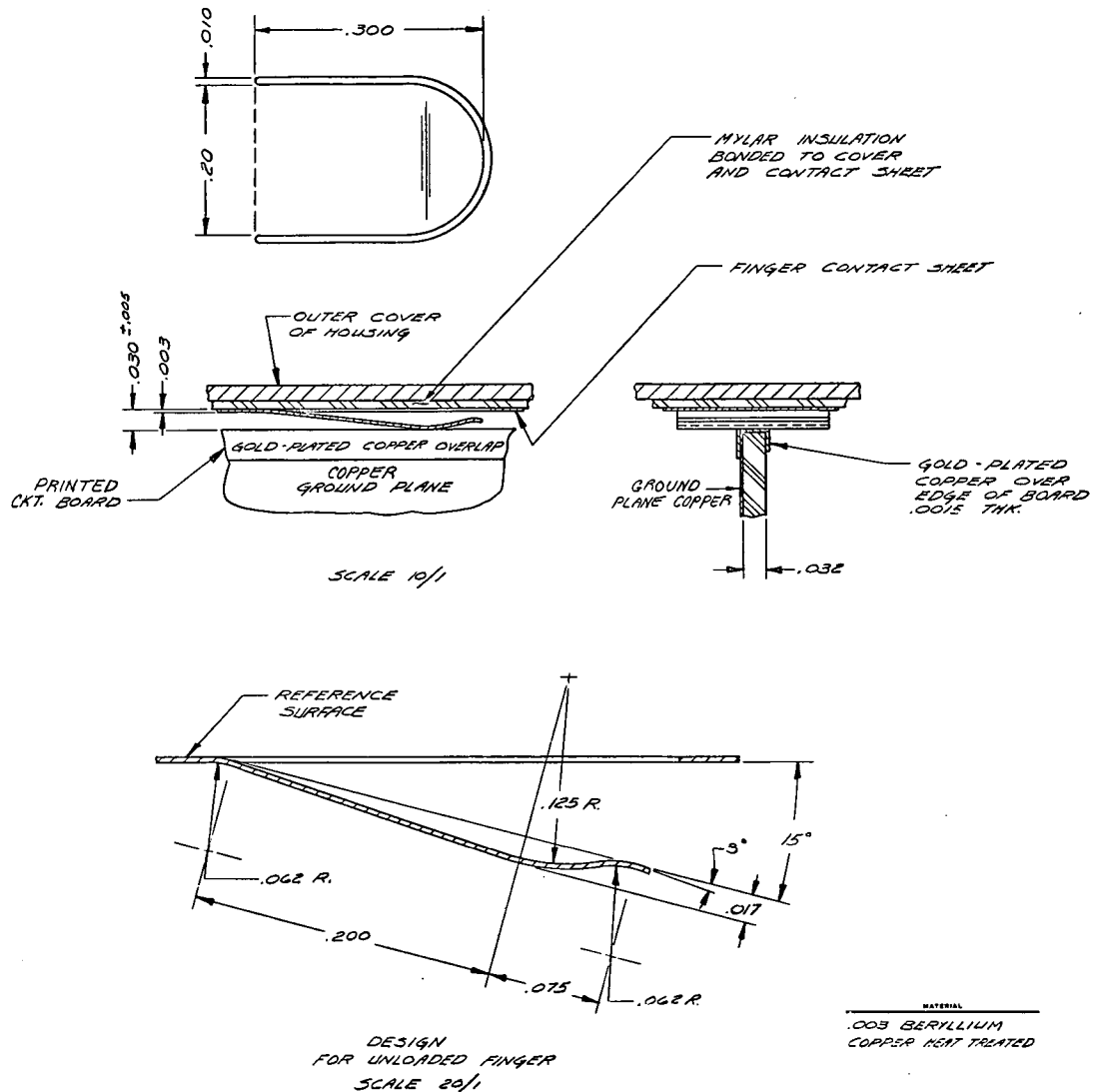


Figure 8. Design of Ground-Plane Finger Contacts

2.3.2 Motherboard Layout. — Many problems arise when a complex electronic system comprising numbers of signal-amplifying and pulse-producing circuits is to be packaged on multiple circuit boards in a small volume. In the IMP-F and -G experiments, the division of the system between motherboards generally followed the direction of signal flow. The compatibility of some portions of the electronics in proximity with others was an important consideration in determining the placement of each subsystem. The sensitive linear system was at the bottom of the stack on motherboards 1 and 2, near the detector. Output drivers and the oscillator bias supplies were put at the top, on boards 5 and 6. Cross talk between components

and between printed-circuit paths on a motherboard, and even from one motherboard to the next, complicated the layout procedure. Sensitive circuits had to be geographically isolated on a given board and signal routing to the terminals handled carefully. Throughout the procedure, efforts were made to minimize the number of interconnecting wires between boards.

Each printed-circuit layout was designed by a draftsman under the guidance of the packaging engineer. The drawings were twice scale and showed the printed-circuit pattern with the positions of components outlined as they would be seen if one could look through the board. All printed-circuit artwork and the assembly drawings were generated from these master layouts. Components were placed for best packaging efficiency and minimum conductor crossover within the guidelines previously discussed. Unavoidable conductor crossovers were made by strap wires on the component side of the board. Axial lead devices were normally placed against the board, but vertical positioning was necessary in some high-density areas. A minimum lead-hole spacing for each type of horizontally mounted component was established which allowed enough length to safely form the lead bends without stressing the part.

Schematic diagrams for the motherboards are included in this report. These, with the block diagram and the brief motherboard descriptions to follow, show how the system is divided among the boards.

Motherboard 1, Figures 9 and 10, comprises the sensitive input networks and linear amplifiers which are driven by the low-level outputs of the five-element detector telescope. Terminal studs are placed along the back edge of the notched portion of the board directly behind the detector mount to keep the interface wiring short. A row of five small, tubular, ceramic capacitors behind the terminal studs couples test pulses from a pulse generator on motherboard 3 into the preamplifiers, in parallel with each detector. Input coupling and bias networks are laid out on the right side of the cutout. The first two linear amplifier stages of all detector channels are located on this board to increase signal levels sufficiently for distribution to other parts of the system.

Motherboard 2, Figures 11 and 12, contains the remainder of the linear system consisting of all the thin-film linear gates, driving amplifiers, and the delay line. The latter was specially designed and fabricated at Bell Telephone Laboratories for minimum size and weight commensurate with high reliability. An electrostatic shield was molded into place over this board during encapsulation for better isolation from the input circuitry on motherboard 1.

Motherboard 3, Figures 13 and 14, contains the internal calibration pulse generator on the left side of the board and the multiplier system on the right. Five miniature coaxial jacks are mounted along the front edge of the board for connection to external calibration-pulse generators through a cutout in the front panel. These had to be recessed within the panel in accordance with spacecraft requirements. The jack-mounting assembly was attached to both the board and front panel at assembly to distribute the insertion forces from the multiple-connector test plug. Small coaxial cables couple the jacks to terminals along the back of the board for distribution to motherboard 1 with the outputs of the internal pulse generator.

Motherboard 4, Figures 15 and 16, is the first full-size board above the detector mount. The apparent sparseness of components in the upper left corner is due to reduced clearance between the top of the mount and the board in this area. The coincidence system and pile-up rejector occupy the entire board. Coincidence discriminators are positioned along the edges to facilitate placement of the trimming potentiometers where they can be reached easily for adjustment with the board in the stack. The thin-film replacements for these can be seen in Figure 15.

Motherboard 5, Figures 17 and 18, contains the five-channel pulse-height analyzer. Here, as on motherboard 4, the discriminators are positioned along the edges to facilitate trimming. Vacant areas in the upper corners of the layout provide for additional gates, to add flexibility for analyzer-system changes.

Motherboard 6, Figures 19 through 21, contains 470 components but no thin-film circuits. Redundant, oscillator-type bias supplies and voltage multipliers are located along the right side of the board, as shown in Figure 19. These supplies are designed to operate above 100 kHz to reduce the size and weight of their components. This permits the use of small, tubular 1000-pF ceramic filter capacitors and miniature toroidal-core transformers (the two molded cubes in the right front corner).

A component at the rear of the board, similar in appearance to the bias transformers, is a five-winding, noise-rejection transformer. All power-supply lines enter the electronic system through this component and, with suitable filter capacitors, it provides protection against external power-line interference. The balance of components on this board comprise the experiment-mode logic decoding tree and diode matrix. Figure 20 shows the printed-circuit side of motherboard 6.

The experiment/spacecraft connector is attached inside the back of the housing just above the rear left corner of motherboard 6. This open area, recognizable by the absence of components, allows space for proper dress of the connector cable.

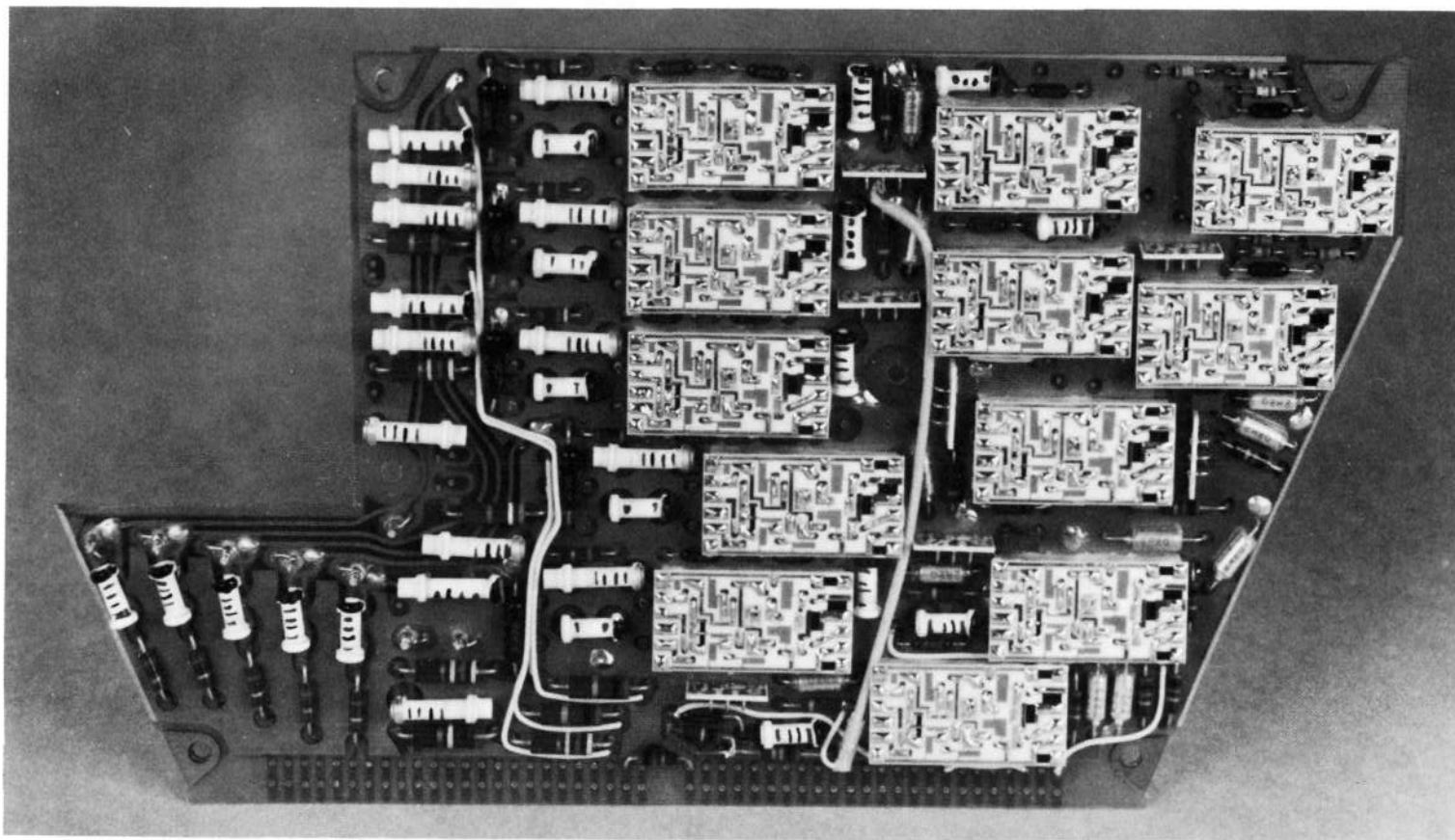
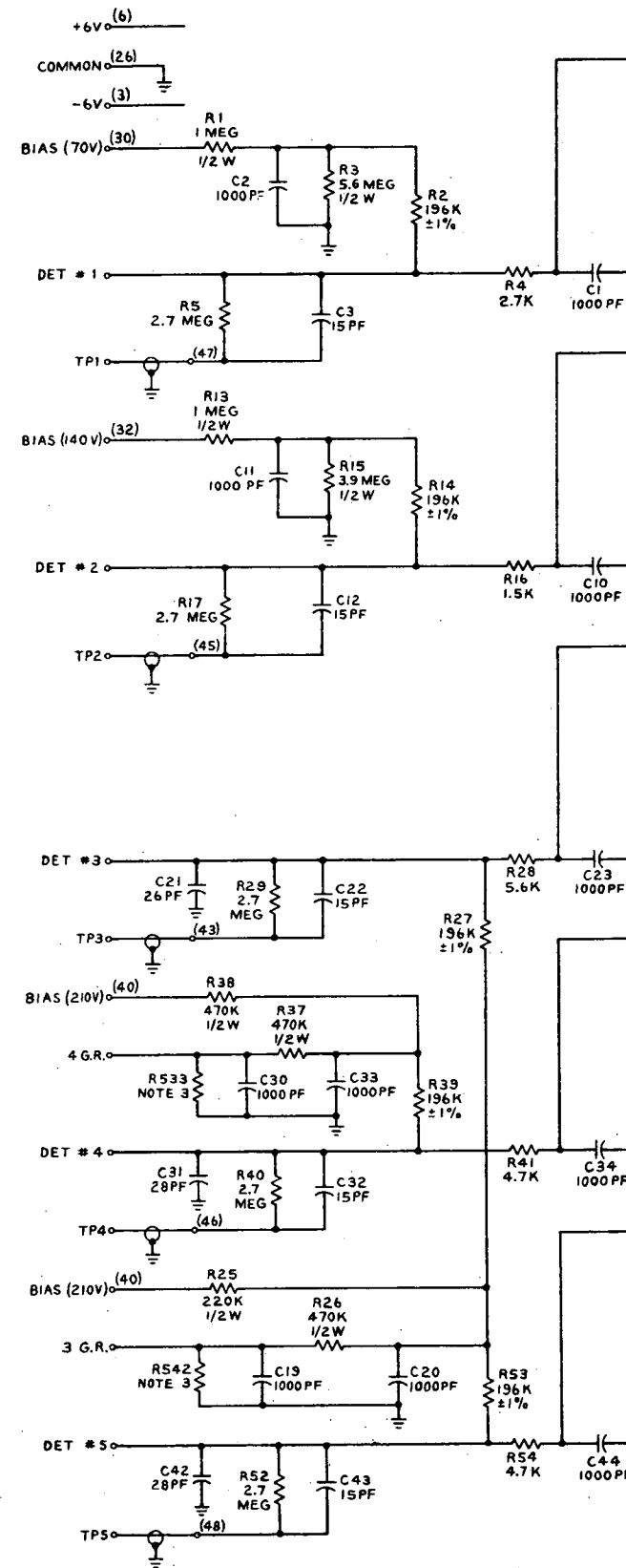
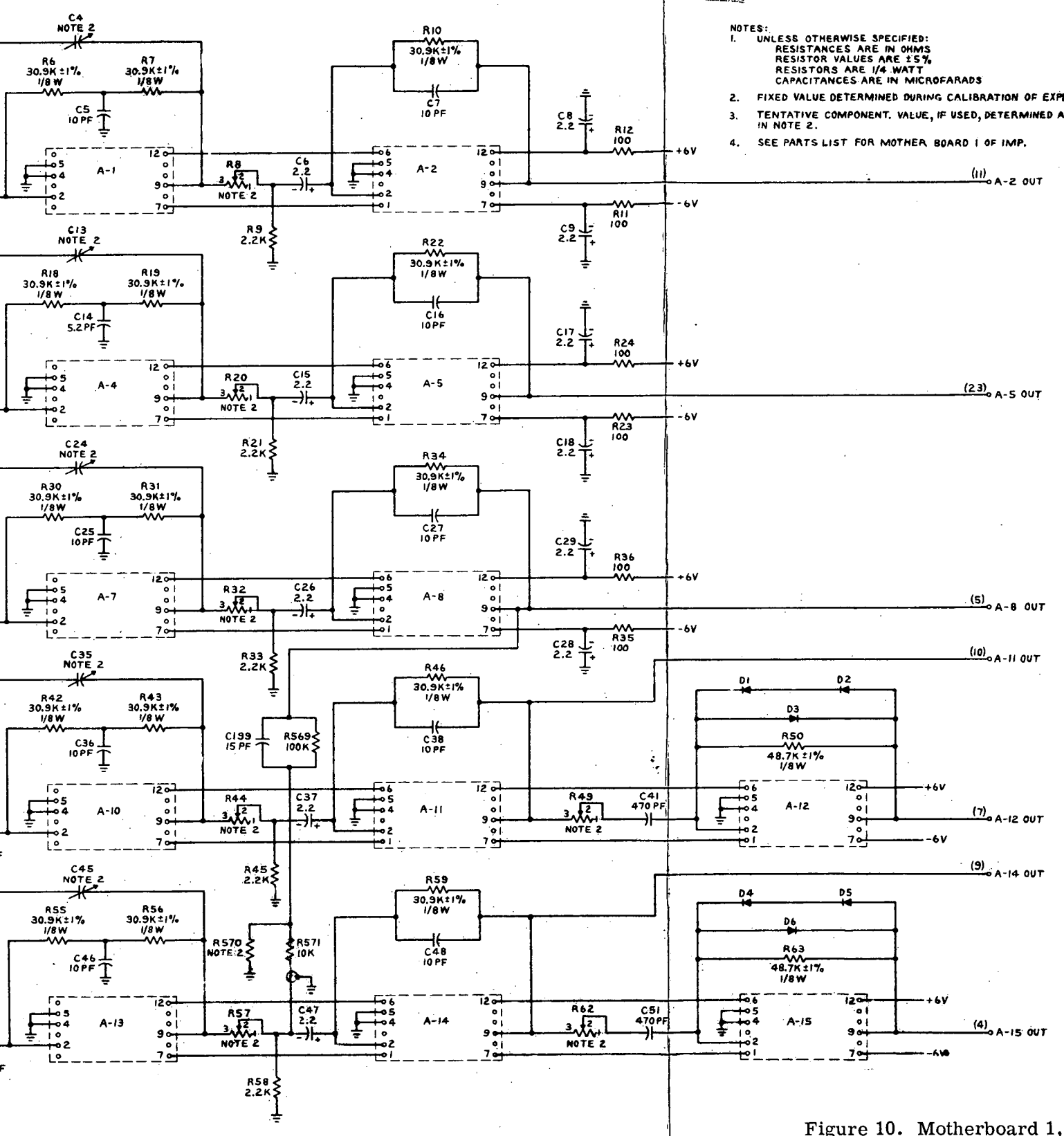


Figure 9. Motherboard 1, Component Assembly

FOLDOUT FRAME 1



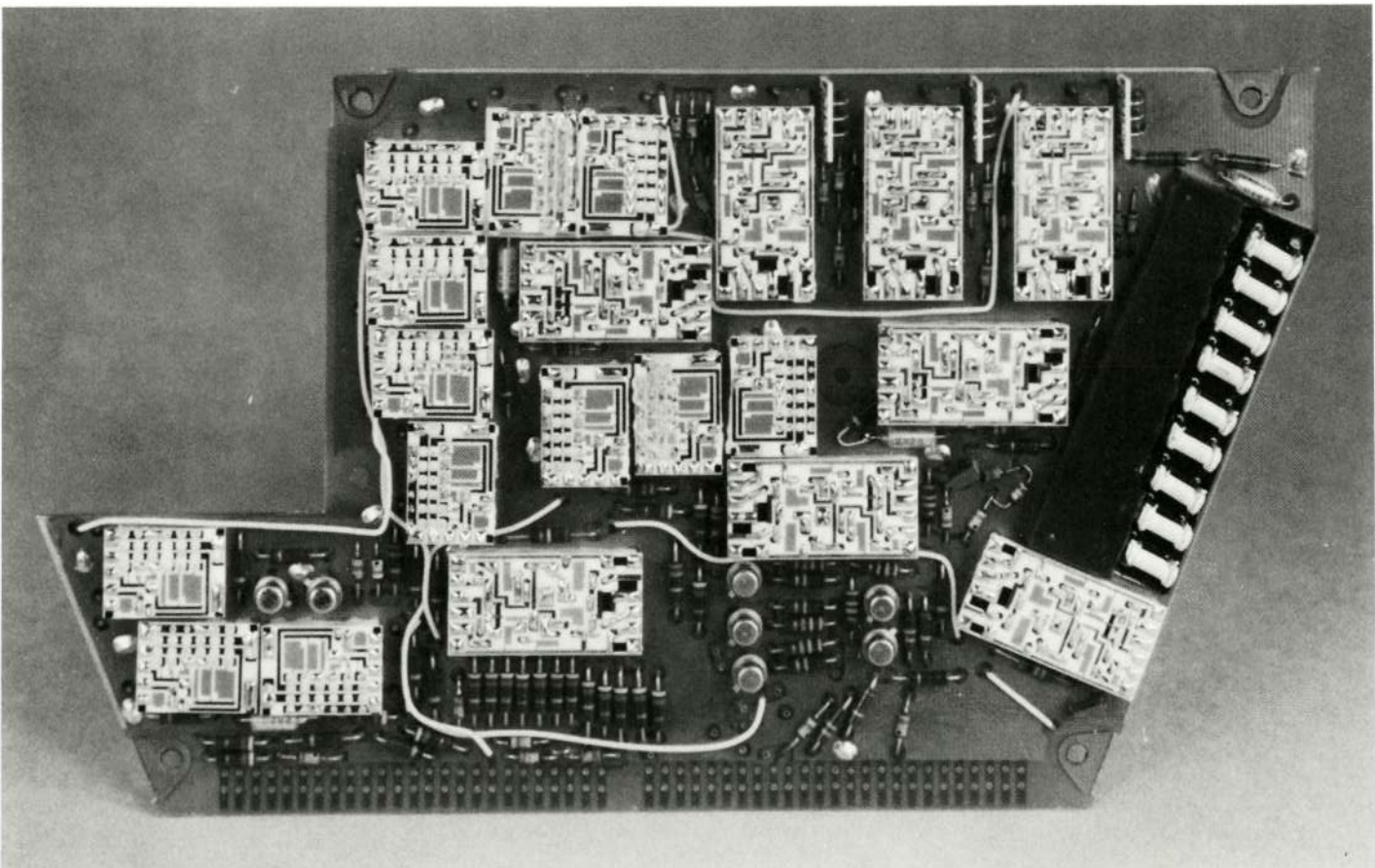
FOLDOUT FRAME 2



- NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTANCES ARE IN OHMS
RESISTOR VALUES ARE $\pm 5\%$
RESISTORS ARE $1/4$ WATT
CAPACITANCES ARE IN MICROFARADS
 2. FIXED VALUE DETERMINED DURING CALIBRATION OF EXPERIMENT.
 3. TENTATIVE COMPONENT VALUE, IF USED, DETERMINED AS DESCRIBED IN NOTE 2.
 4. SEE PARTS LIST FOR MOTHER BOARD 1 OF IMP.

Figure 10. Motherboard 1,
Schematic Diagram

PRECEDING PAGE MATERIAL NOT FILMED



Preceding page blank

Figure 11. Motherboard 2, Component Assembly

PRECEDING PAGE BLANK NOT FILMED

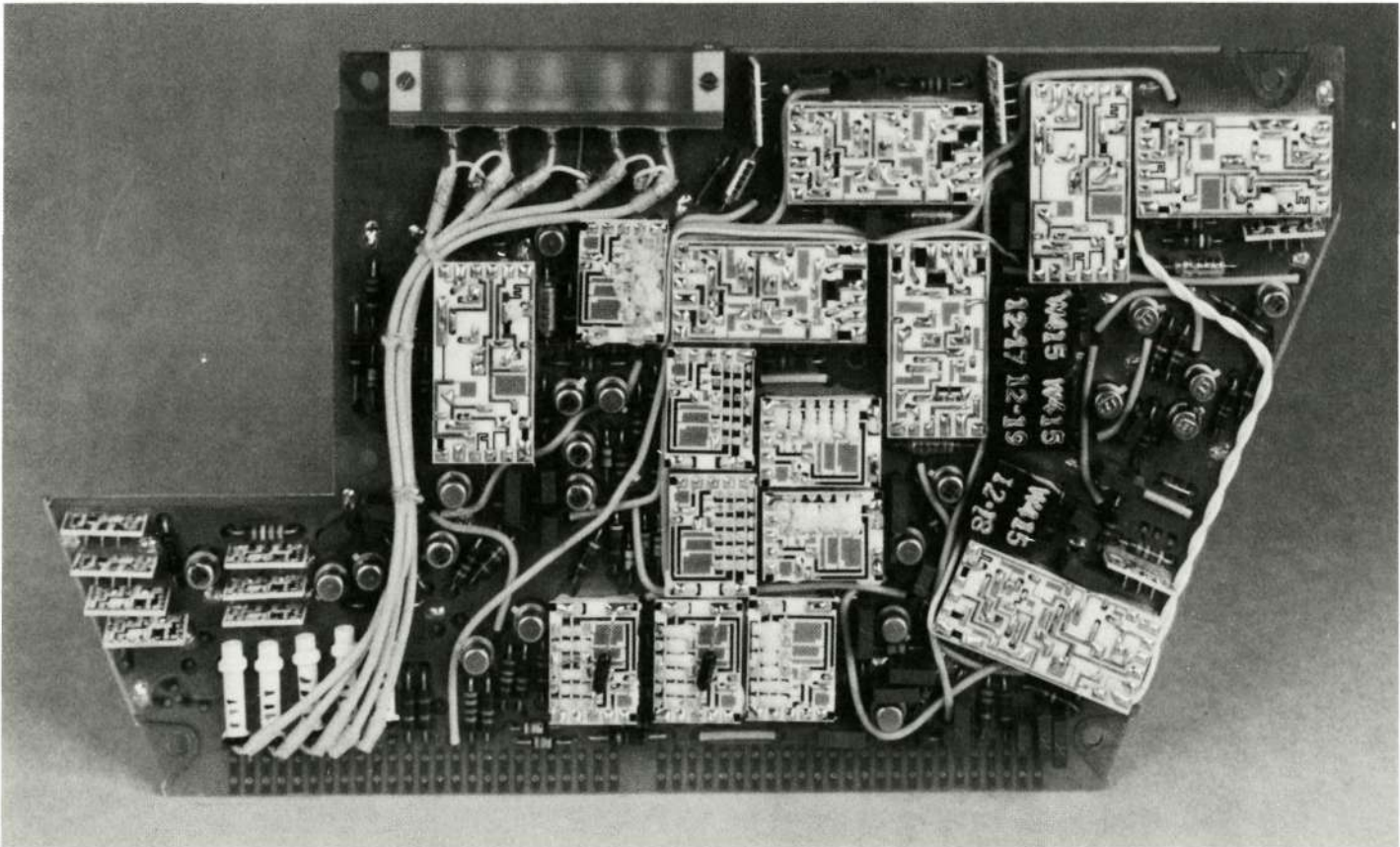


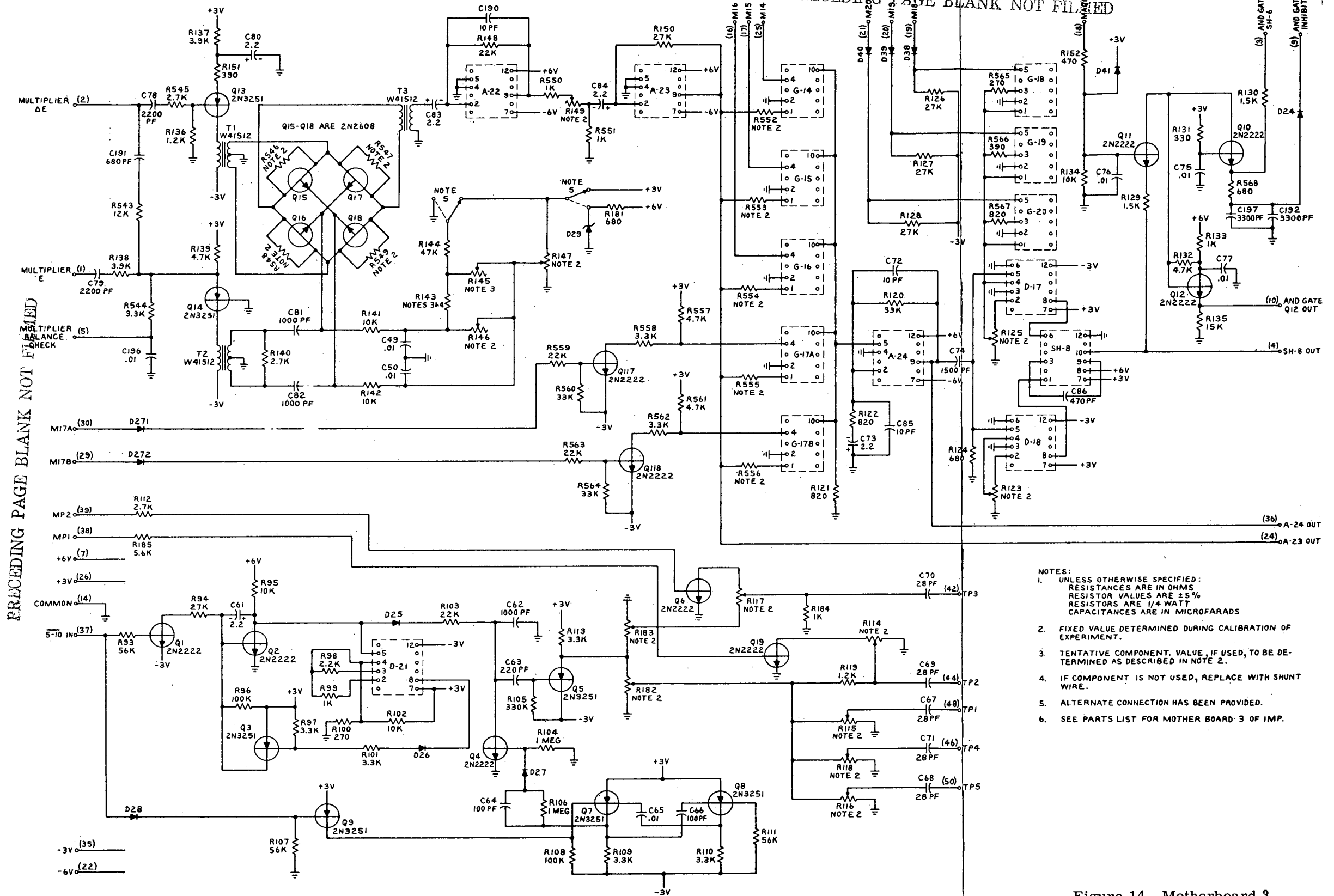
Figure 13. Motherboard 3, Component Assembly

Preceding page blank

FOLDOUT FRAME 1

FOLDOUT FRAME 2

PRECEDING PAGE BLANK NOT FILLED



- NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTANCES ARE IN OHMS
RESISTOR VALUES ARE $\pm 5\%$
RESISTORS ARE 1/4 WATT
CAPACITANCES ARE IN MICROFARADS
 2. FIXED VALUE DETERMINED DURING CALIBRATION OF EXPERIMENT.
 3. TENTATIVE COMPONENT VALUE, IF USED, TO BE DETERMINED AS DESCRIBED IN NOTE 2.
 4. IF COMPONENT IS NOT USED, REPLACE WITH SHUNT WIRE.
 5. ALTERNATE CONNECTION HAS BEEN PROVIDED.
 6. SEE PARTS LIST FOR MOTHER BOARD 3 OF IMP.

Preceding page blank

Figure 14. Motherboard 3,
Schematic Diagram

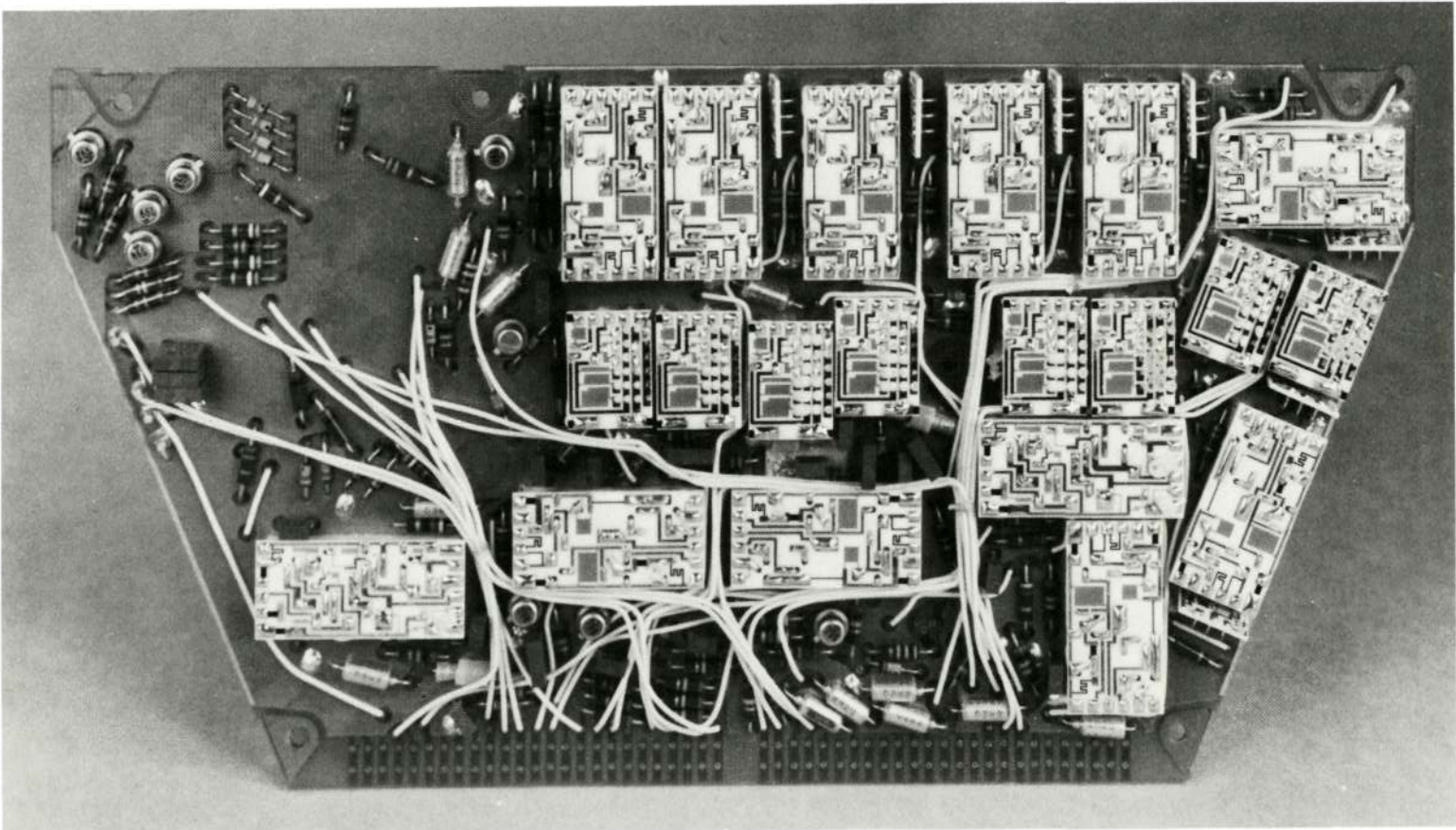
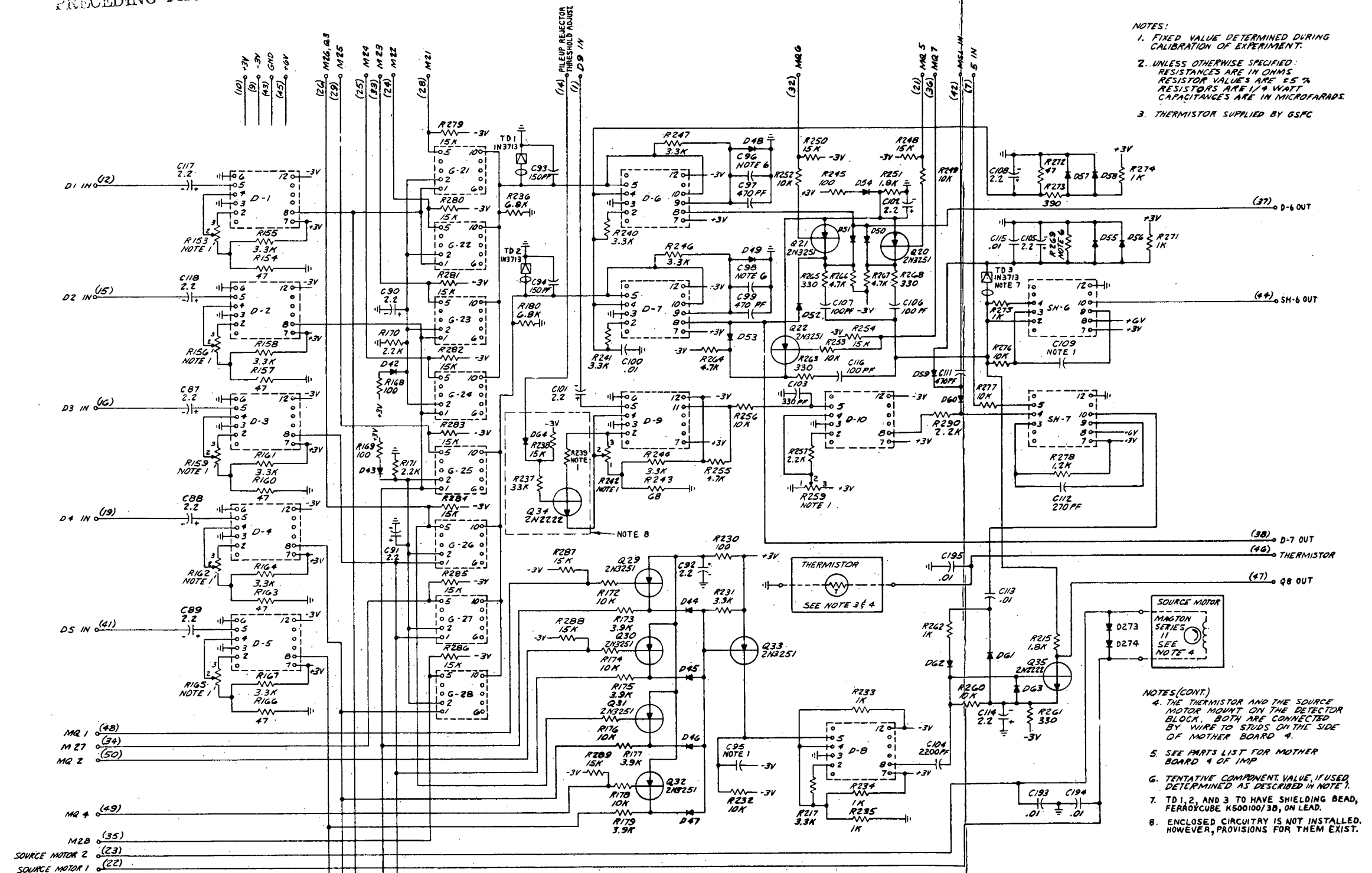


Figure 15. Motherboard 4, Component Assembly

Preceding page blank

FOLDOUT FRAME

PRECEDING PAGE BLANK NOT FILMED



FOLDOUT FRAME 2

Figure 16. Motherboard 4, Schematic Diagram

Preceding page blank

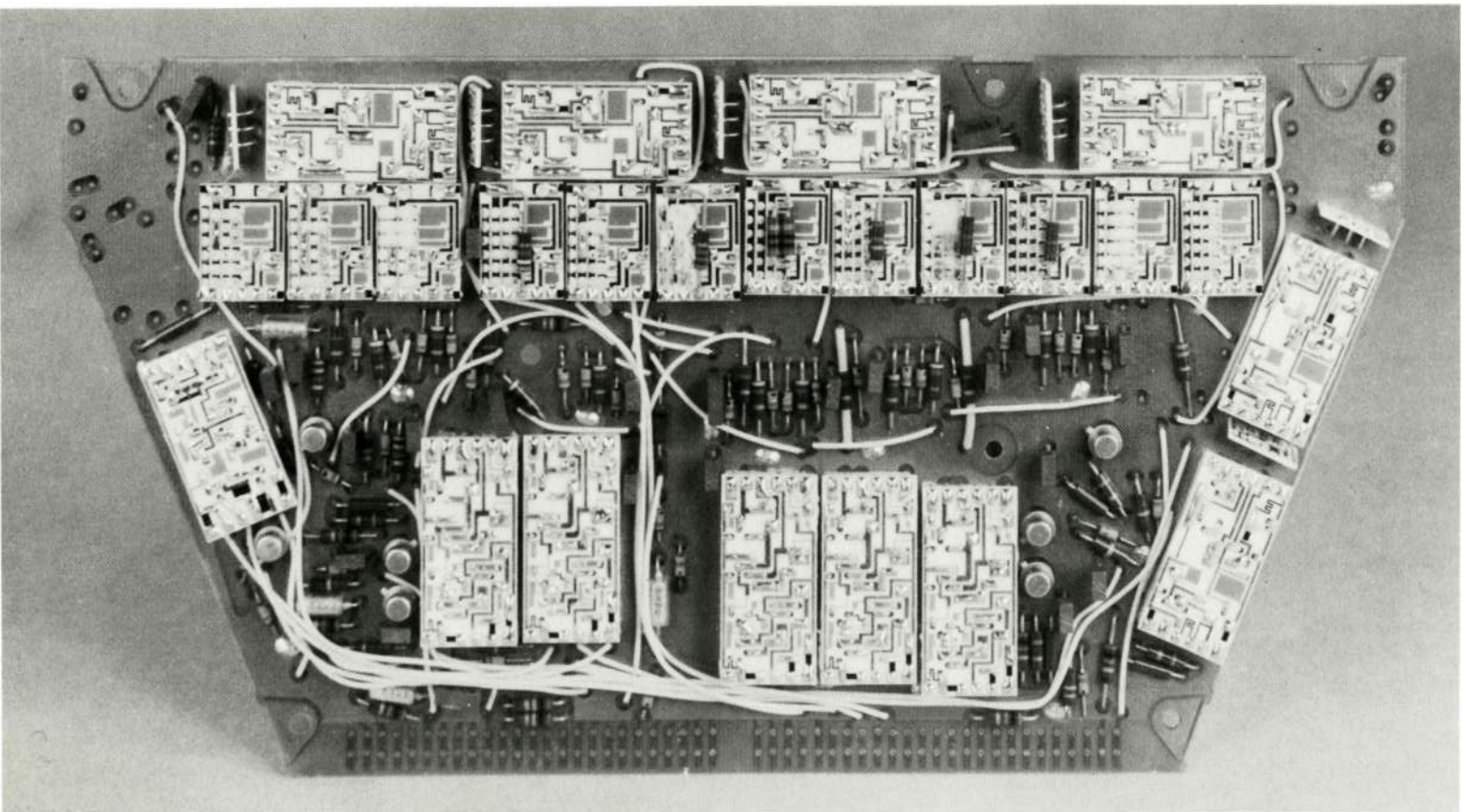


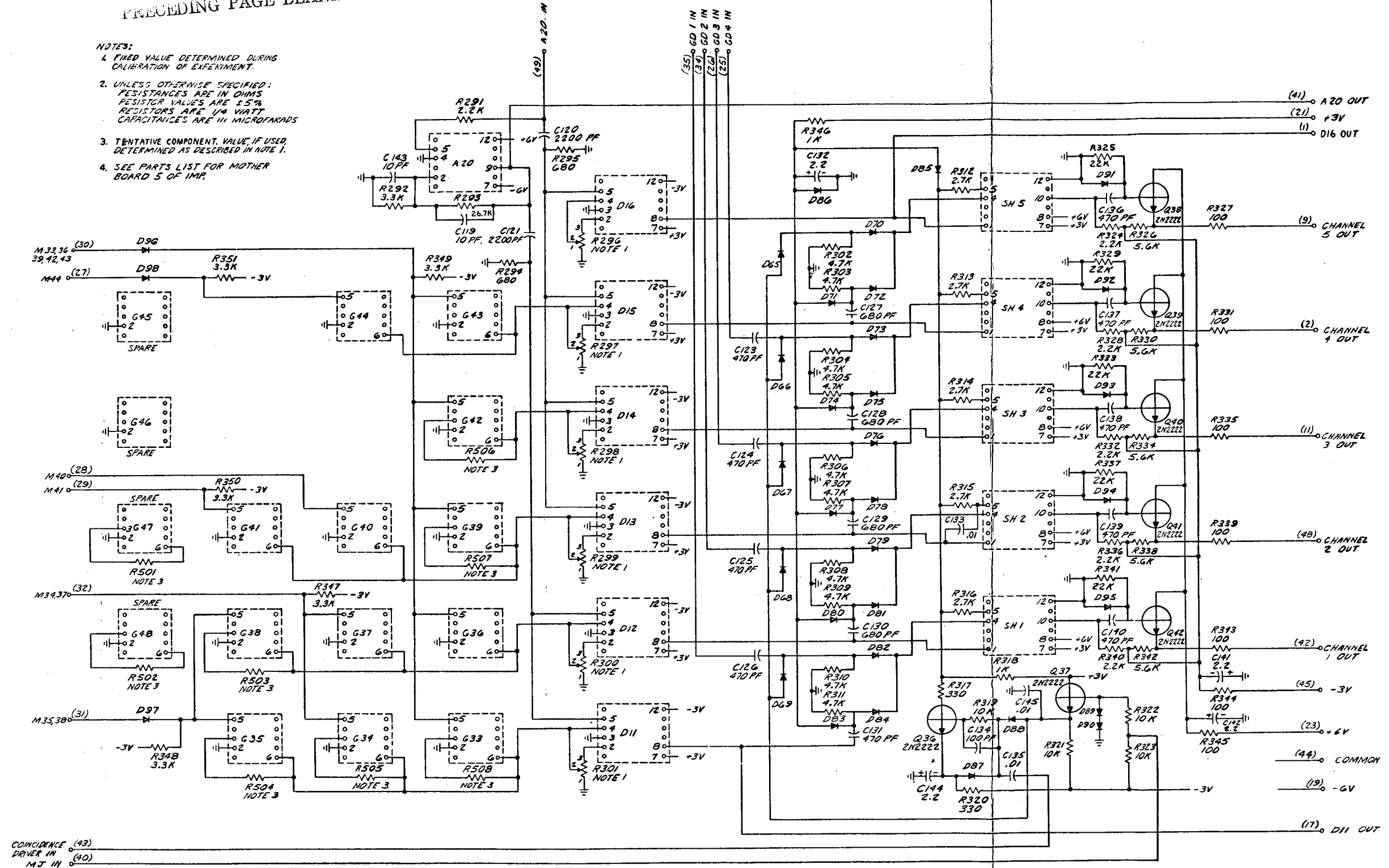
Figure 17. Motherboard 5, Component Assembly

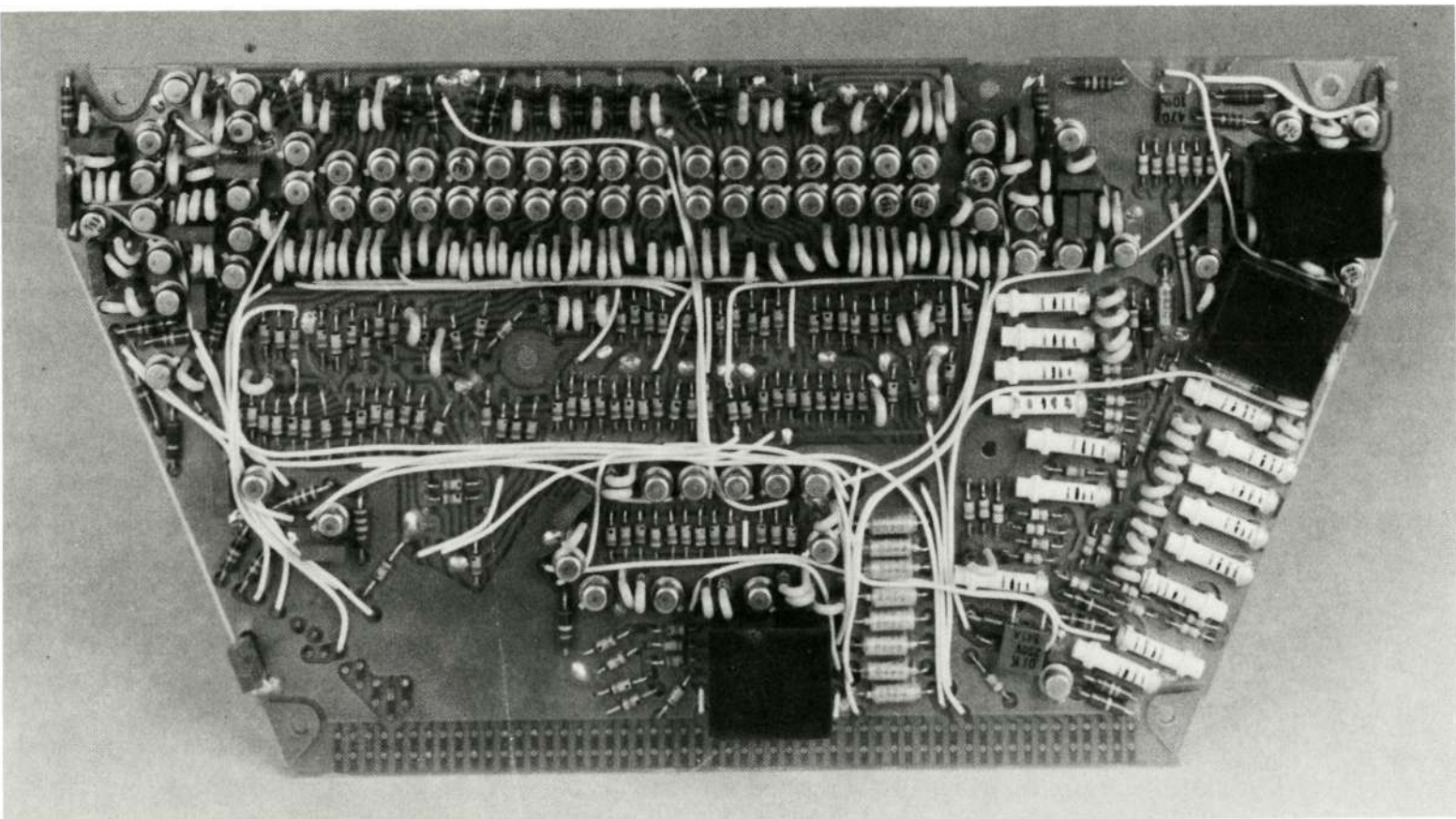
Preceding page blank

FOLDOUT FRAME 1
PRECEDING PAGE BLANK NOT FILMED

FOLDOUT FRAME

- NOTES:
1. FIXED VALUE DETERMINED DURING CALIBRATION OF EXPERIMENT.
 2. UNLESS OTHERWISE SPECIFIED: RESISTANCES ARE IN OHMS. RESISTOR VALUES ARE 15%. RESISTORS ARE 1/4 WATT. CAPACITANCES ARE IN MICROFARADS.
 3. TENTATIVE COMPONENT VALUE, IF USED DETERMINED AS DESCRIBED IN NOTE 1.
 4. SEE PARTS LIST FOR MOTHER BOARD 5 OF IMP.





Preceding page blank

Figure 19. Motherboard 6, Component Assembly

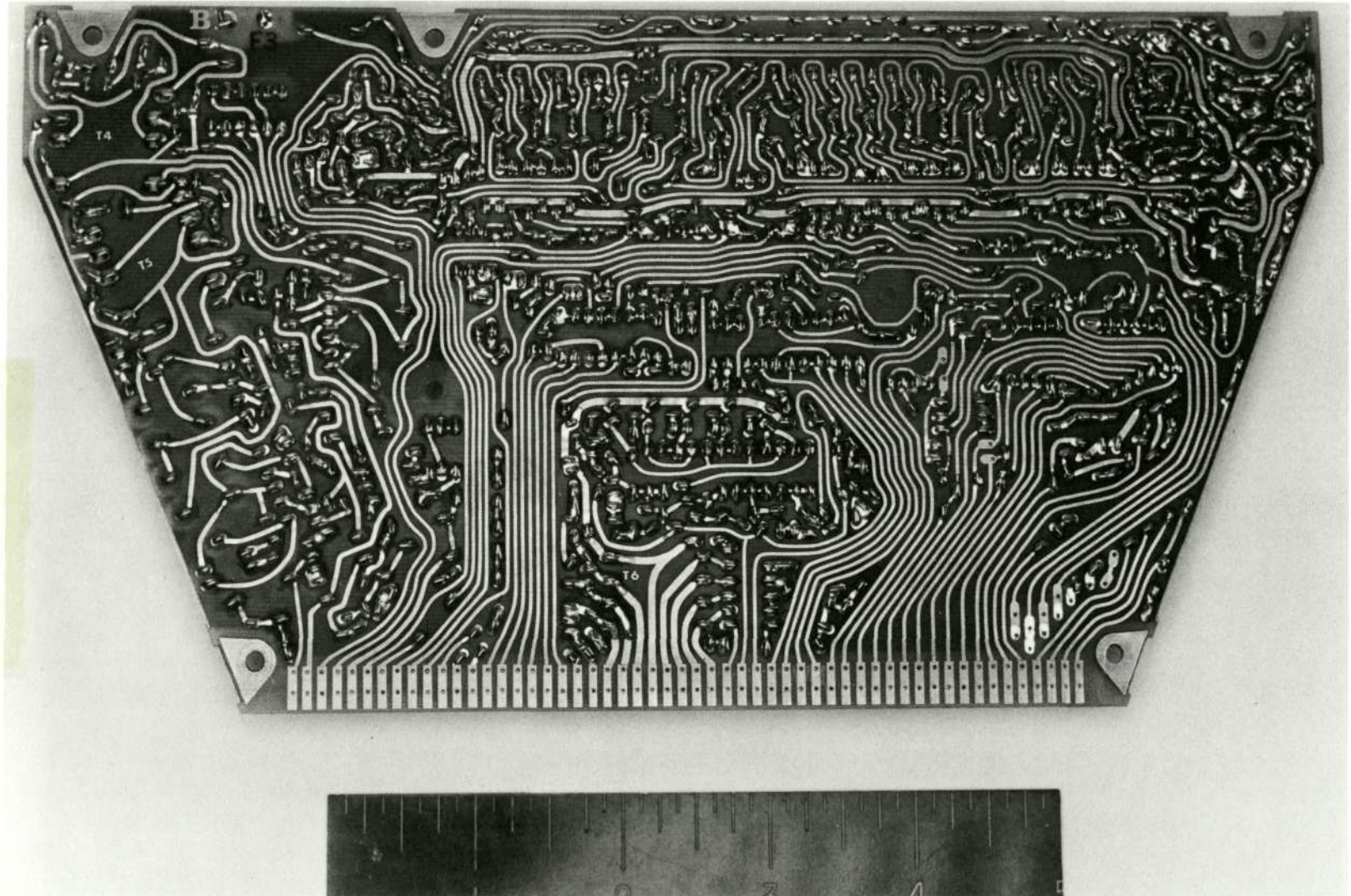
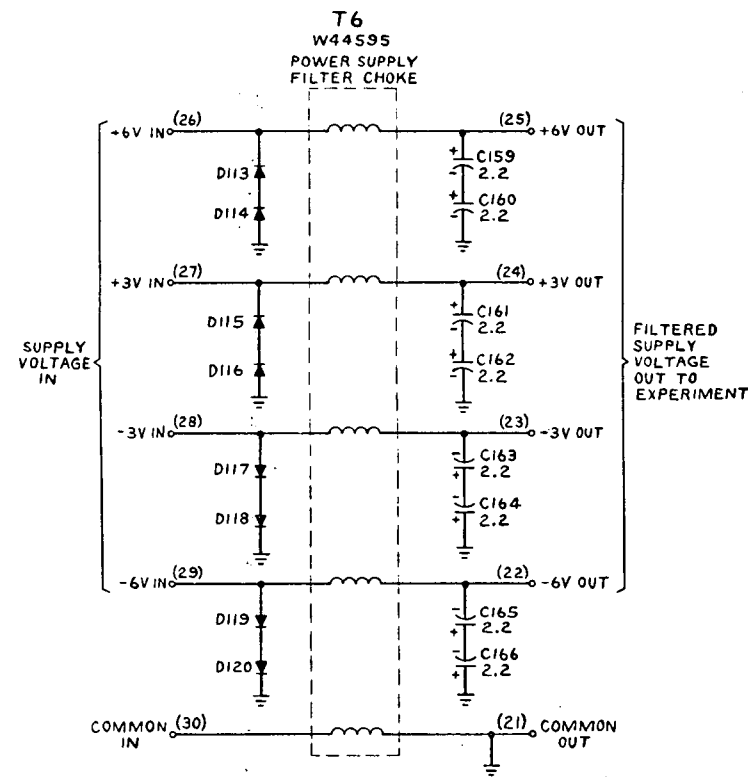


Figure 20. Motherboard 6, Printed Circuit

FOLDOUT FRAME



- NOTES:
1. UNLESS OTHERWISE SPECIFIED:
RESISTANCES ARE IN OHMS
RESISTOR VALUES ARE $\pm 5\%$
RESISTORS ARE 1/4 WATT
CAPACITANCES ARE IN MICROFARADS
 2. FIXED VALUE DETERMINED DURING CALIBRATION OF
EXPERIMENT.
 3. SEE PARTS LIST FOR MOTHER BOARD 6 OF IMP.

41.1

FOLDOUT FRAME

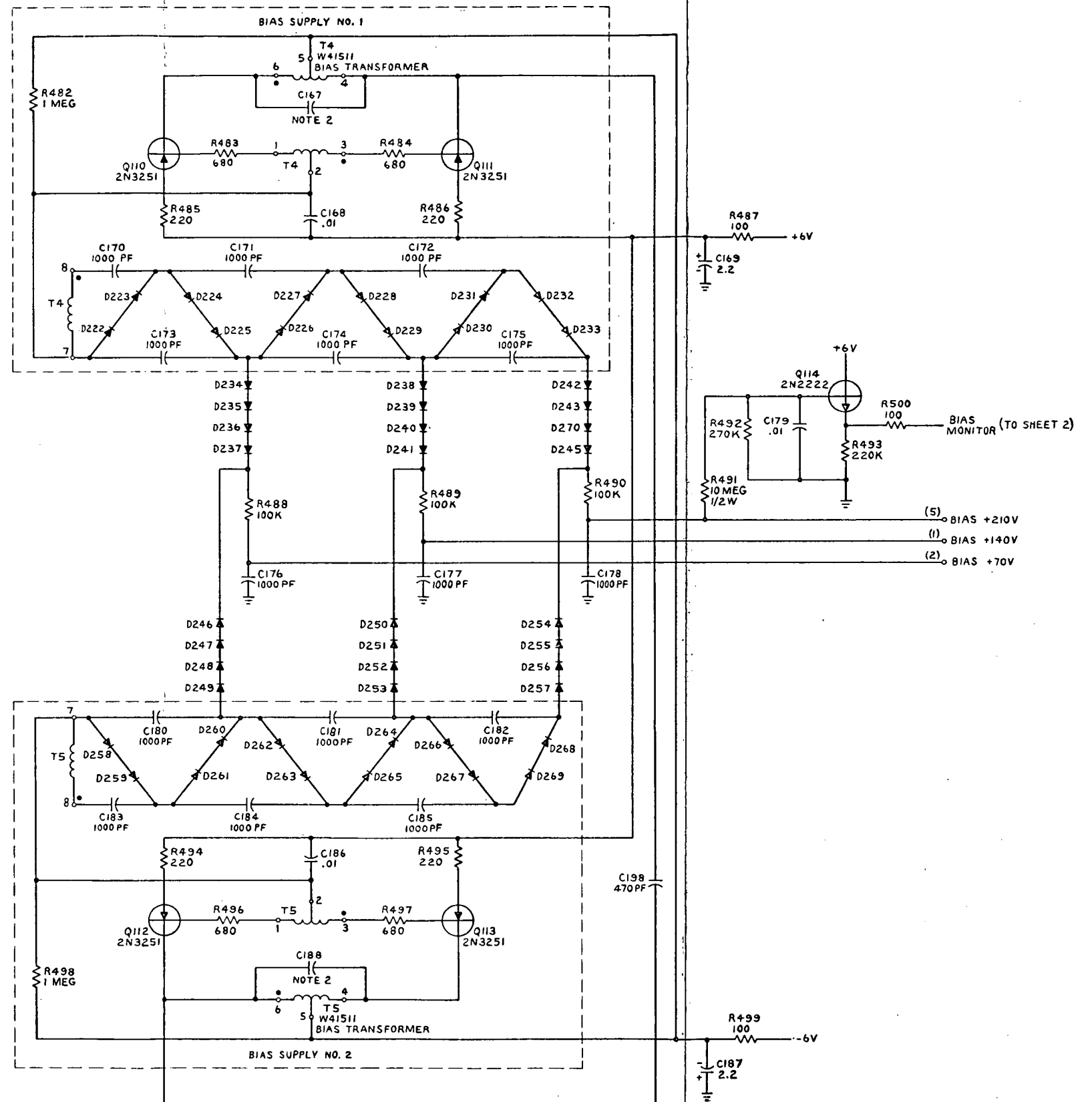


Figure 21. Motherboard 6, Schematic Diagram (Sheet 1 of 3)

41.2

FOLDOUT FRAME 1
PRECEDING PAGE BLANK NOT FILMED

FOLDOUT FRAME 2

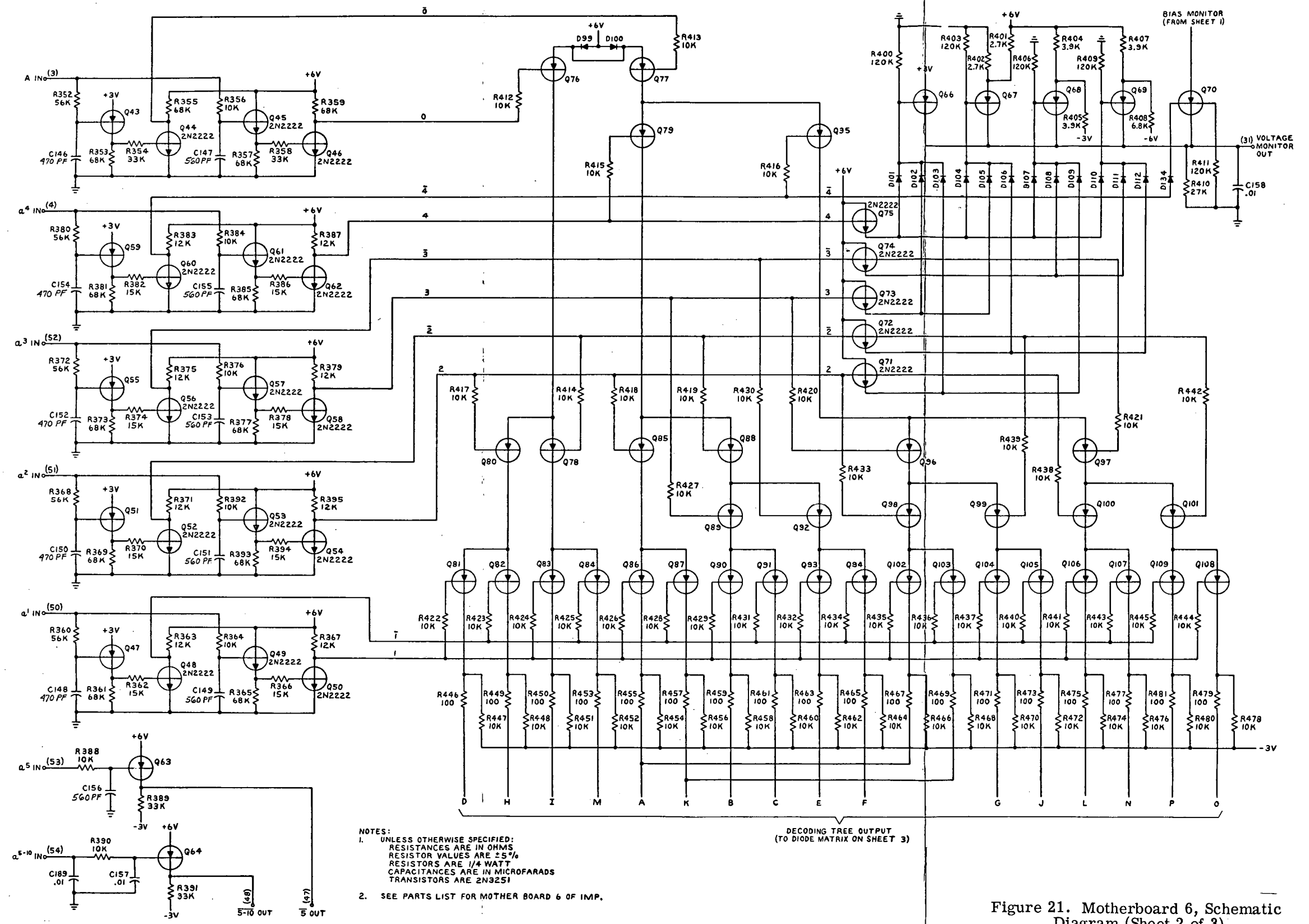


Figure 21. Motherboard 6, Schematic Diagram (Sheet 2 of 3)

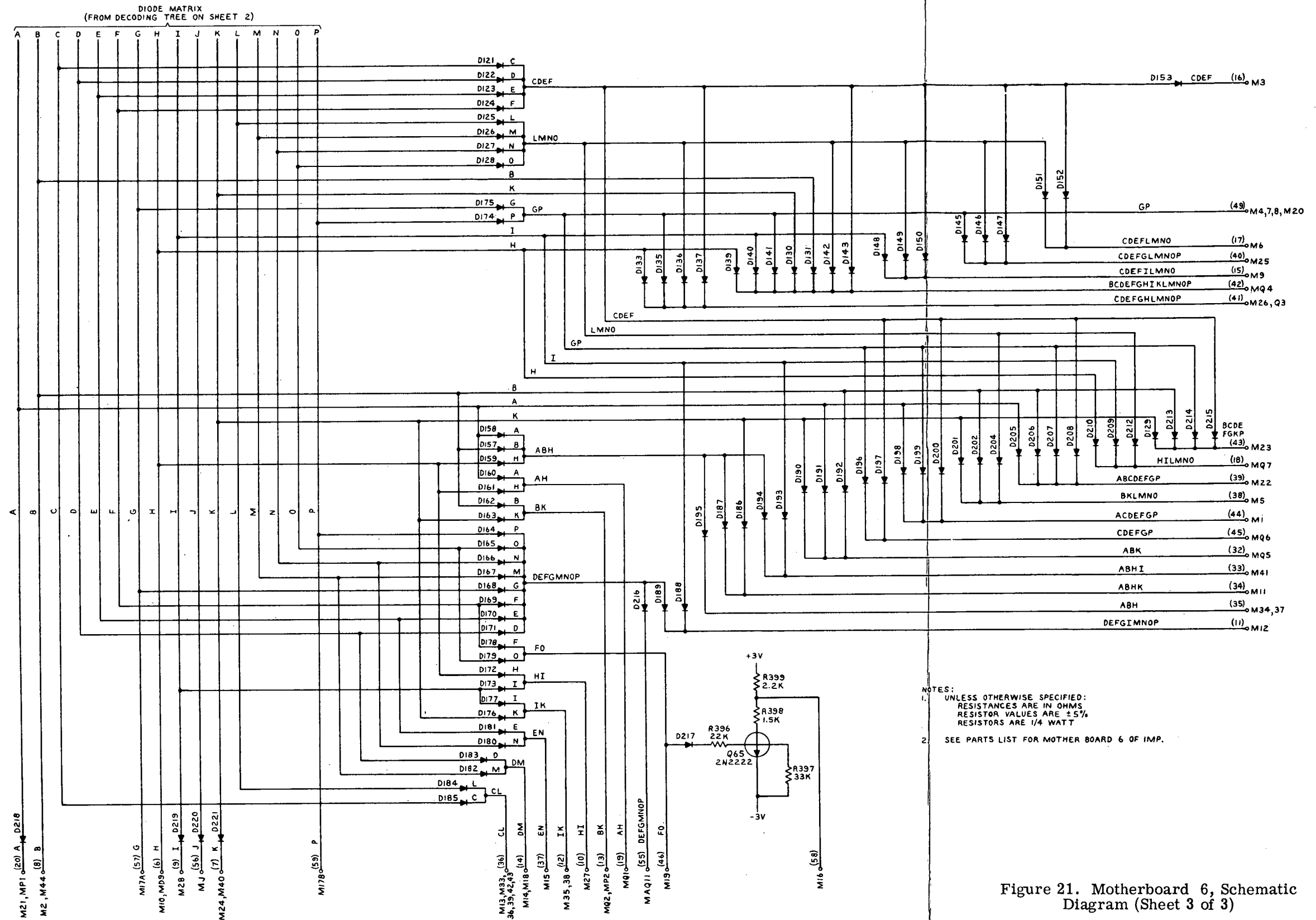
Preceding page blank

43.1

43.2

FOLDOUT FRAME 1
PRECEDING PAGE BLANK NOT FILMED

FOLDOUT FRAME 2



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
RESISTANCES ARE IN OHMS
RESISTOR VALUES ARE $\pm 5\%$
RESISTORS ARE 1/4 WATT
2. SEE PARTS LIST FOR MOTHER BOARD 6 OF IMP.

Figure 21. Motherboard 6, Schematic
Diagram (Sheet 3 of 3)

Preceding page blank

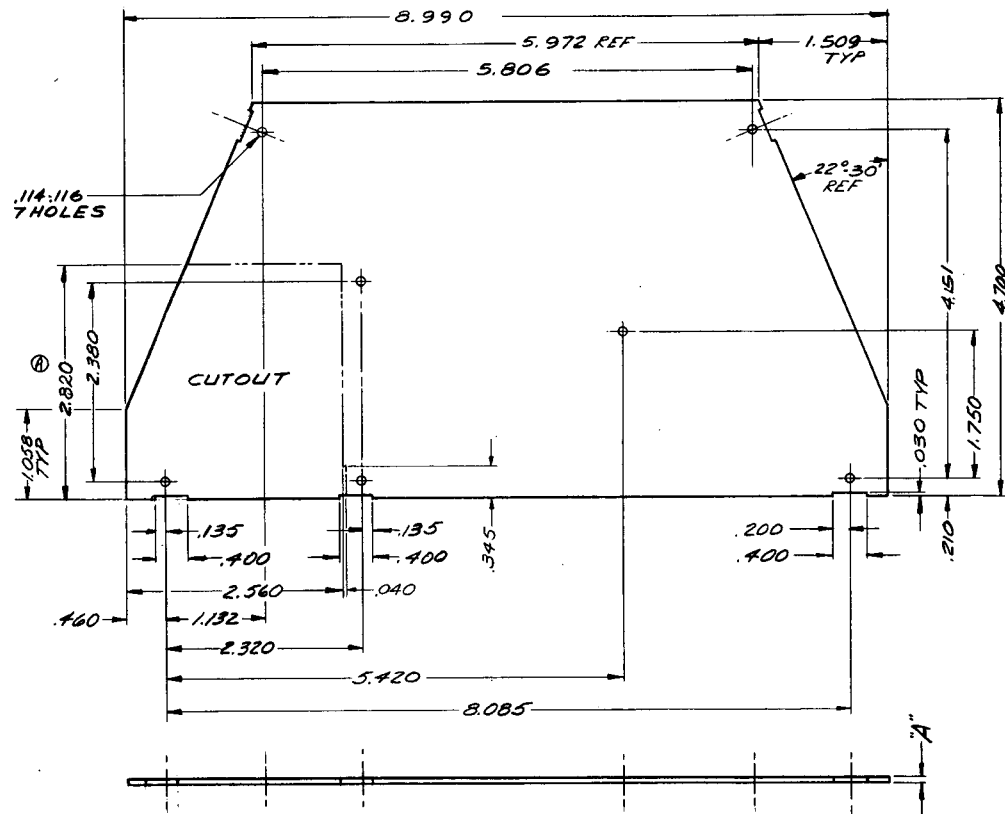
45.1

45.2

2.4 Electronic Stack Design

2.4.1 Physical Description. — A dimensional drawing of the motherboards is shown in Figure 22. The boards are slightly smaller than the inner dimensions of the housing, to provide a gap at the front and sides for proper operation of the ground-plane contact fingers. An 0.25-inch gap between the rear edge and the housing back plate accommodates the harness wires.

The separation between boards was determined by tubular aluminum spacers located at each of the 0.114-inch-diameter through-bolt holes shown on the board drawing. Interboard spacing within the stack is typically 0.5 inch; this increases to 0.65 inch between boards 1 and 2 to provide clearance for extra shielding. The



PART NO.	DIM 'A'	CUTOUT	MATERIAL
B-615724 -1	.040	WITHOUT	FIBERGLASS EPOXY
B-615724 -3	.040	WITH	FIBERGLASS EPOXY

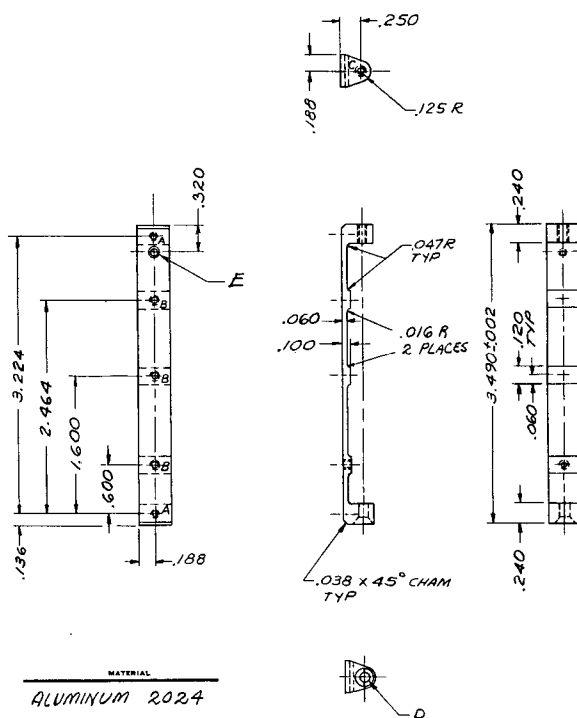
Figure 22. Motherboard Dimensions

Preceding page blank

stack is inverted at motherboard 5 so that the components on both end boards face outward. Since the printed circuits on boards 4 and 5 face each other, the spacing between them is 0.24 inch.

Figure 23 shows the design of the stack brackets. These provide an anchor for the through-bolts but do not actually sustain any of the compressive forces on the stack. For this reason, and to conserve weight, nominal bracket thickness was held to 0.060 inch; heavier bosses for the threaded mounting-screw holes were positioned to lie within the gaps between circuit boards. The ends were thicker in order to support the through-bolts. Each bracket was attached to the stack of boards at assembly by inserting a through-bolt at the countersunk end and passing it through all circuit boards and spacers beginning at motherboard 1 until it exited just above

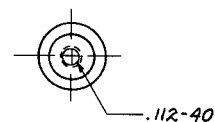
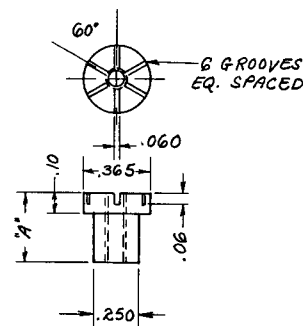
motherboard 6. After a flat washer was placed over the bolt end, a special castellated nut, shown in Figure 24, was screwed on loosely. The bolt was then run up into the threaded top end of the bracket until it was just snug. Then the castellated nut was tightened firmly against motherboard 6, compressing the whole stack of spacers



NOTES:
1. DRILL THESE HOLES AT
ASSY.

HOLE	DESCRIPTION	REQ
A	2-56 X .150 DP (NOTE 1)	2
B	3-48 (NOTE 1)	3
C	4-40	1
D	.114-.116 DIA & CSK 80°-82° TO .226-.228	
E	.060-80, CSK FOR SCREWS SUPPLIED	1

Figure 23. Motherboard Stack Bracket



DIM. A
.280

MATERIAL
ALUMINUM

Figure 24. Castellated Nut for Circuit-Board Clamping

and boards. As the nut was tightened, one of the six grooves on the nut turret was brought into alignment with a small threaded hole at the top of the bracket. A 0-80 flathead screw inserted in the hole and passing through both bracket and groove prevents the nut from loosening during vibration. These castellated nuts were used because the layout and density of components on motherboard 6 precluded the use of a hex-nut wrench. A special pronged tool, pivoting in the through-bolt hole in the top bracket, was used to tighten the nuts from above.

2.4.2 Encapsulation Technique. — Polyurethane foam was chosen as the best encapsulant, in view of the high vibration levels specified. The use of foam in earlier experiments had the serious disadvantage of restricting access to the electronics for troubleshooting, repairs, and modifications. However, much of this hardship was due to a practice of encapsulating the entire electronic package with the housing. In the IMP-F and -G experiments, this problem was overcome by foaming the component side of each circuit board separately and leaving the printed-circuit side exposed for testing. By a procedure described in paragraph 4.4.3, the height of the foam layer on each board was adjusted to 0.01 inch less than the length of the aluminum spacers. Under compression in the assembled stack, solder connections on the printed-circuit side of each board were pressed into the foam on the next board. The result was a large area of contact between boards, which greatly increased the mechanical integrity of the whole package.

All exposed wiring was encapsulated with a silicone rubber foam, described in paragraph 4.6. This material remained flexible after cure, permitting the circuit boards to be fanned apart without destroying the encapsulant.

2.5 Detector Mount Design

Figure 2 shows a cutaway drawing of the basic detector mount and detector-telescope cartridge assembly. The function of the mount is threefold:

- (1) Radiation shielding for the detector, to reduce its background counting rate from the rear and sides.
- (2) Mechanical support for the detector cartridge, socket, and associated hardware.
- (3) Electrical shielding for the cartridge and its terminations.

For simplicity, the outer details of the IMP-F and -G mount are not shown on the basic drawing.

The mount assembly comprises

- (a) a ceramic socket at the rear, fitted with vacuum-tube-type pin receptacles;
- (b) an insulated, concentric sleeve shield which surrounds both detector cartridge and socket to prevent noise pulses on the detector mount (chassis ground) from coupling to the detector cartridge and leads;
- (c) a shielded back plate which, with the concentric shield, completes the electrostatic shielding of the detector socket;
- (d) the collimator, a ribbed cylinder in front of the detector, designed to reduce scattering of particles in the detector aperture; and
- (e) the front ring, containing a 20-degree shielded entrance cone and the titanium foil window.

A special tool was used to insert the detector cartridge into the mount.⁴ A thick ceramic insulating washer, followed by a phosphor bronze spring washer, was placed in front of the cartridge before the collimator was installed. The threaded front ring was then torqued against the collimator and cartridge to 35 inch-pounds to prevent movement of any of the components during vibration.

The engineering drawing of the IMP-F and -G detector mount is shown in Figure 25. To save weight, the mount was machined over most of its length to the smallest circular cross section which would still provide adequate shielding for the detector (exclusion of protons below 30 MeV). The semaphore-type aluminum arm, which carries two radioactive calibration sources in its flag end,⁴ operates in a narrow slot cut in the left side of the mount. With the arm in retracted position, the sources are effectively shielded from the detector by the corner of the mount. The rotary solenoid mechanism which actuates the arm is attached to a boss behind the slot. This assembly is shown in the photograph of the electronic stack in Figure 4. The mount is gold-plated to protect its aluminum surfaces and to maintain good electrical conductivity.

For protection against vibration, the detector mount is located in one corner of the housing to take advantage of support from both the front plate and left side. It is also securely interlocked with the electronic stack in the following ways:

- (a) by a modified, flanged stack bracket, screwed to the front right side of the mount;
- (b) by a through-bolt, in a tab at the rear right corner, which goes through the height of the stack and into a threaded bushing on motherboard 6 (shown in Section B-B, Figure 5);

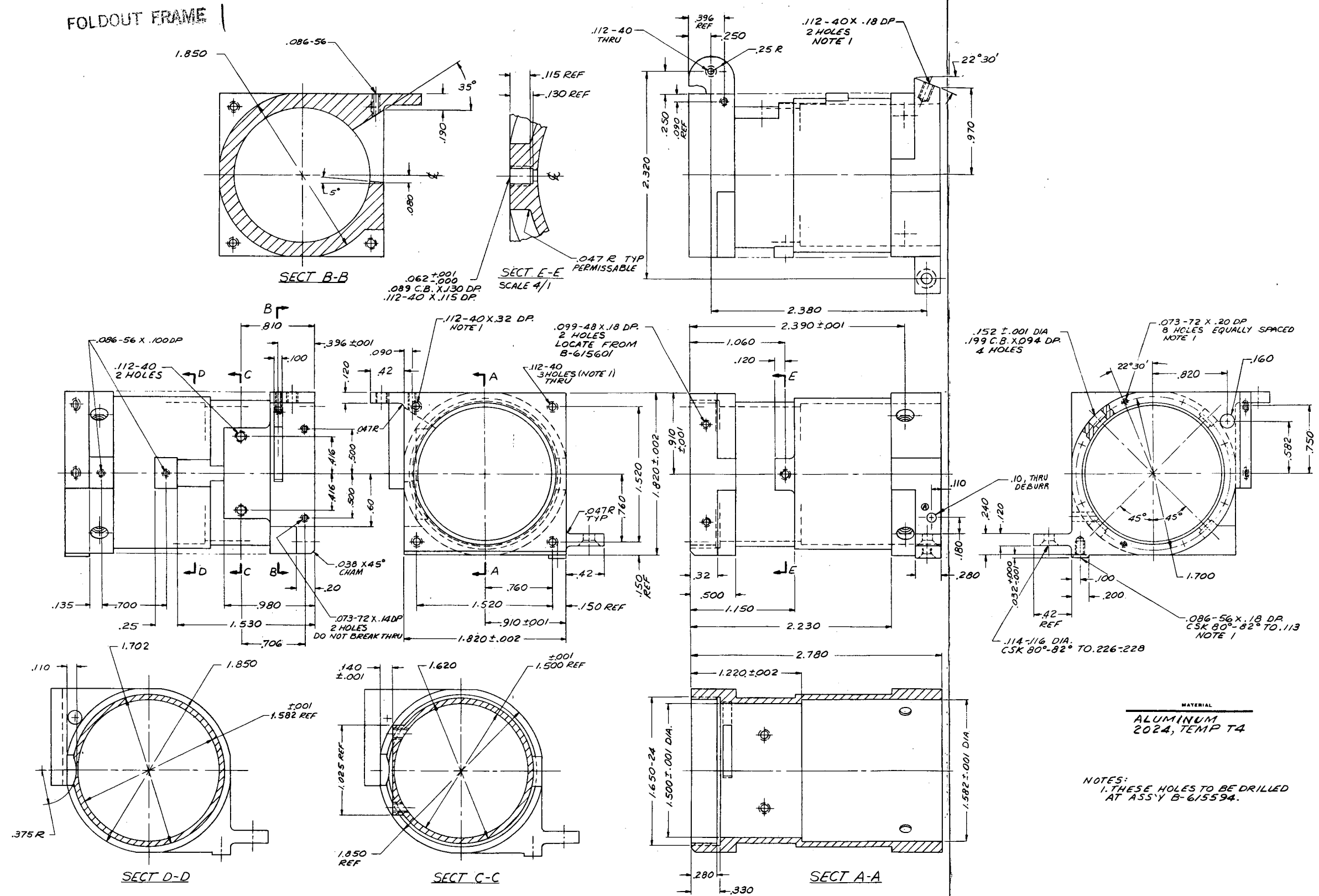


Figure 25. IMP-F and -G Detector Mount

51.1

51.2

- (c) by a short bolt running down through the left corners of motherboards 6, 5, and 4 into a threaded tab in the upper front left corner of the mount (shown in Section A-A, Figure 5). This also secures the front left corners of the top three full-width motherboards.

Figure 26 shows the detector-mount back plate. Grooves were machined in a raised portion along one side edge to engage and support the outer corners of the cutouts in motherboards 1, 2, and 3. When the plate was screwed in place on the back of the mount, a copper disc on its inner surface made electrical contact with the exposed end of the concentric ground shield.

2.6 Housing

Goddard Space Flight Center supplied housings to all experimenters for Projects IMP-F and -G in an effort to minimize spacecraft mechanical integration problems. These housings were normally fabricated as open, riveted frames conforming to the basic IMP-F and -G module outline. The recommended procedure was to assemble

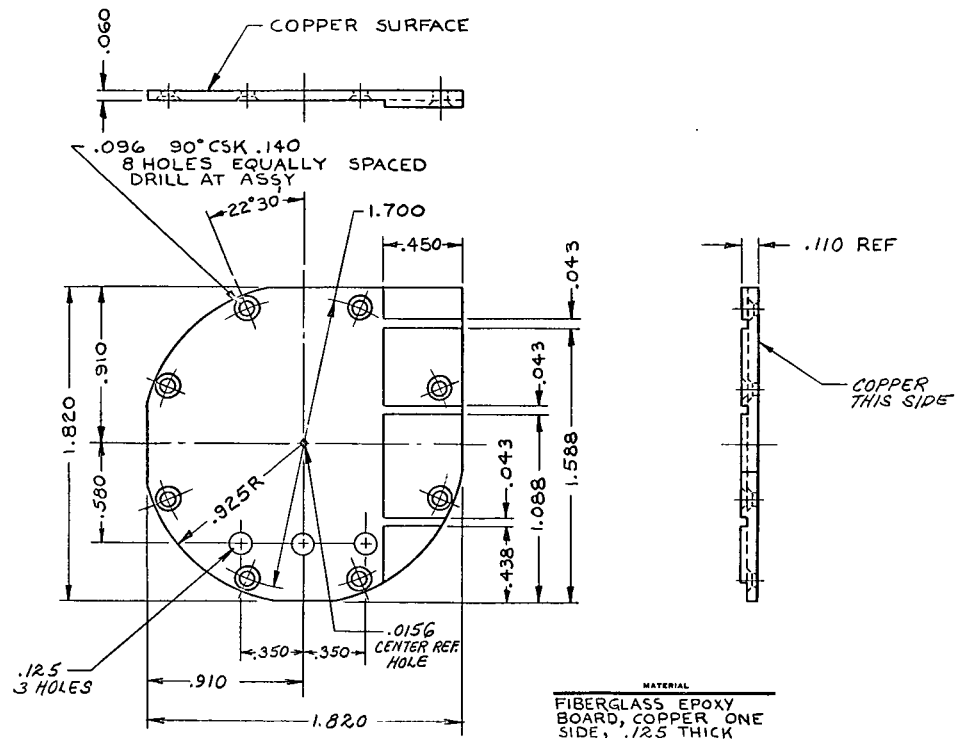


Figure 26. Detector-Mount Back Plate

Preceding page blank

the experiment within the frame and pot it in place with polyurethane foam. As mentioned in paragraph 2.4, this technique has the serious disadvantage of limiting access to an experiment whose electronics is packaged in a stack of circuit boards. Upon special request to NASA, the housing frame was supplied to Bell Laboratories as four separate details. A major problem with this procedure was the correct alignment of the experiment mounting holes located in each corner. This was overcome by performing all fitting and assembly operations at BTL on an assembly jig which accurately simulated spacecraft mounting conditions.

The housing-assembly drawing is given in Figure 27. All details were fabricated from 0.032-inch-thick aluminum sheet. The surfaces were anodized black, except in overlapping areas where it was necessary to preserve electrical continuity between parts. The front and rear members were stiffened by bending a 1/4-inch lip along their top and bottom edges. Flanges at each end of these pieces provided a means for attaching the sides.

Stiffness of the side members was increased, to improve fingerstock contact, by forming ribs into the metal. The ends of the side members were rolled into 0.24-inch-diameter tubes through which the spacecraft mounting bolts were inserted in each corner of the assembled housing.

Stake nuts were installed in various locations on the members for mounting screws. Cutouts on the front plate were made for the detector and test jacks; the smaller opening was keyed to prevent accidental insertion of the wrong test connector.

Covers were not normally provided for the IMP-F and -G module frames. However, it was essential that the electronics for the BTL experiments be shielded against external interference. Figures 28 and 29 show the top and bottom cover designs. To conserve weight, these covers were made from 0.020-inch-thick aluminum.

FOLDOUT FRAME 2

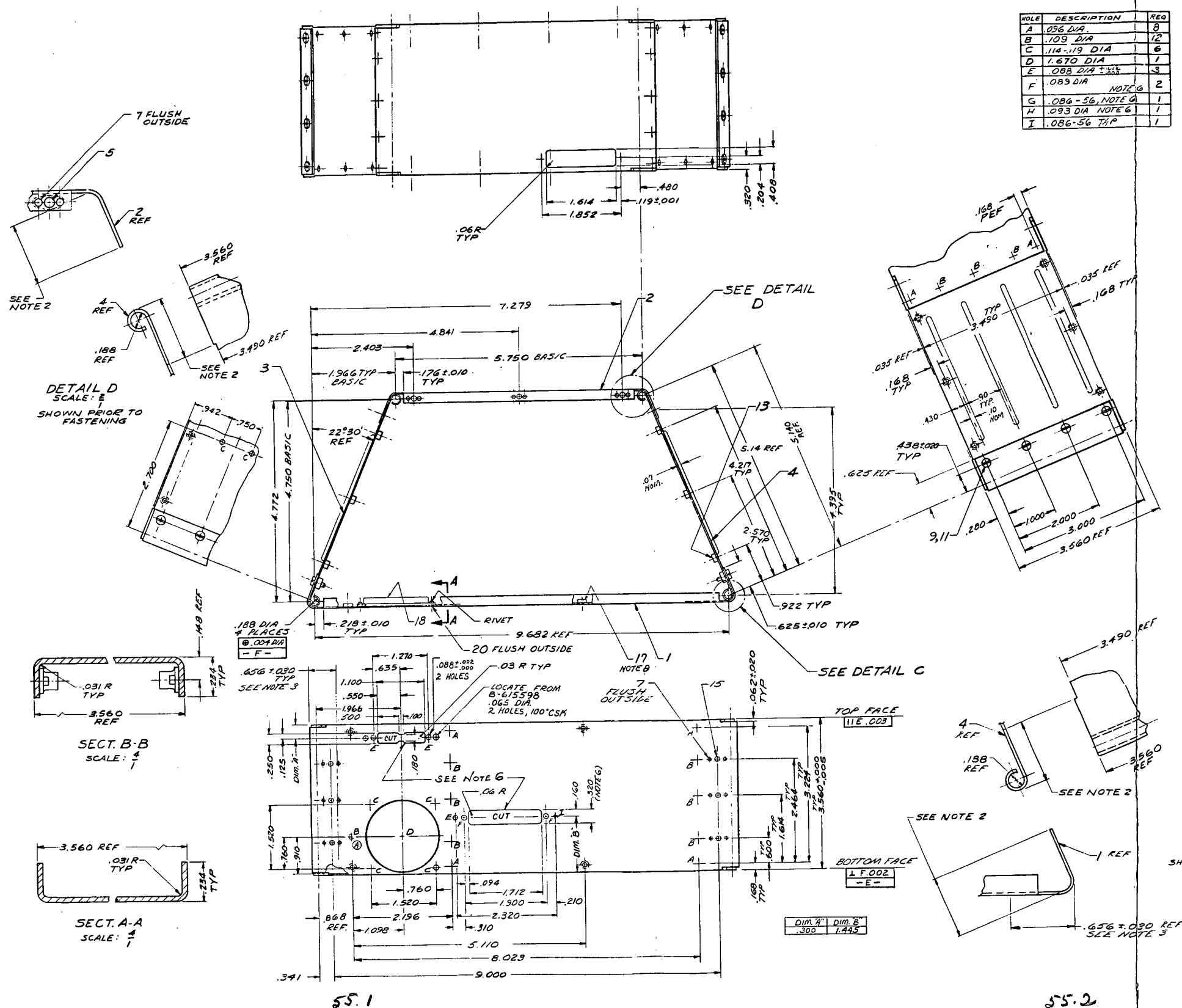
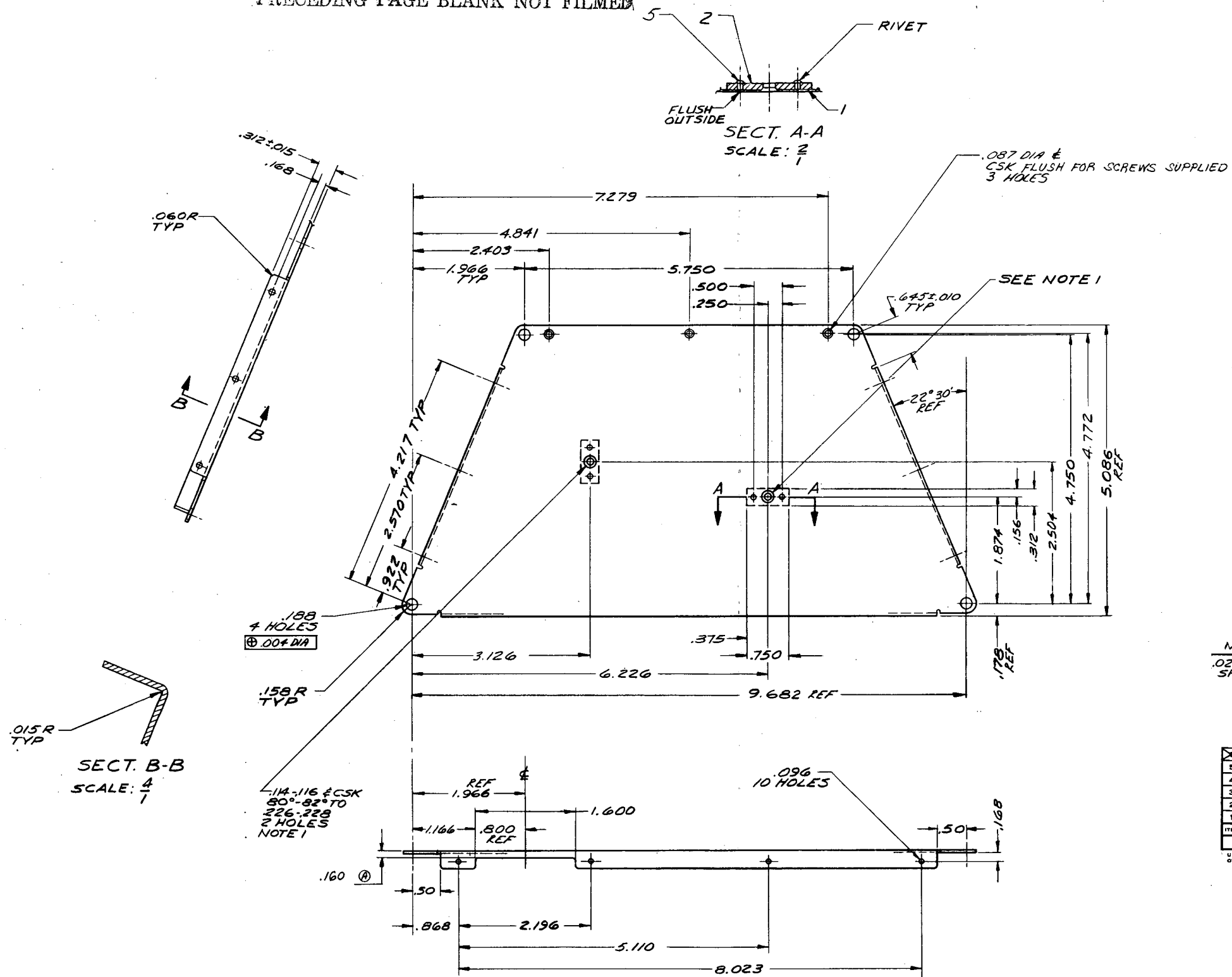


Figure 27. Housing Assembly

PRECEDING PAGE BLANK NOT FILMED



NOTES:

1. THESE HOLES TO BE DRILLED BY BTL. AT ASSY.
2. REMOVE BURRS & BREAK SHARP EDGES.
3. ANODIZE IN ACCORDANCE WITH MIL-A-8625,
TYPE II, DYE BLACK.

MATERIAL ITEM 1	MATERIAL ITEM 2
.020 ALUMINUM SHEET 6061-T6	.060 ALUMINUM SHEET 6061-T6

5		RIVET, FLAT HD 100°CSK	
4		1/16 DIA X.125LG. AL-2024	4
3			
2		PLATE	2
1		COVER	1
ITEM	PIECE	NAME	REQ

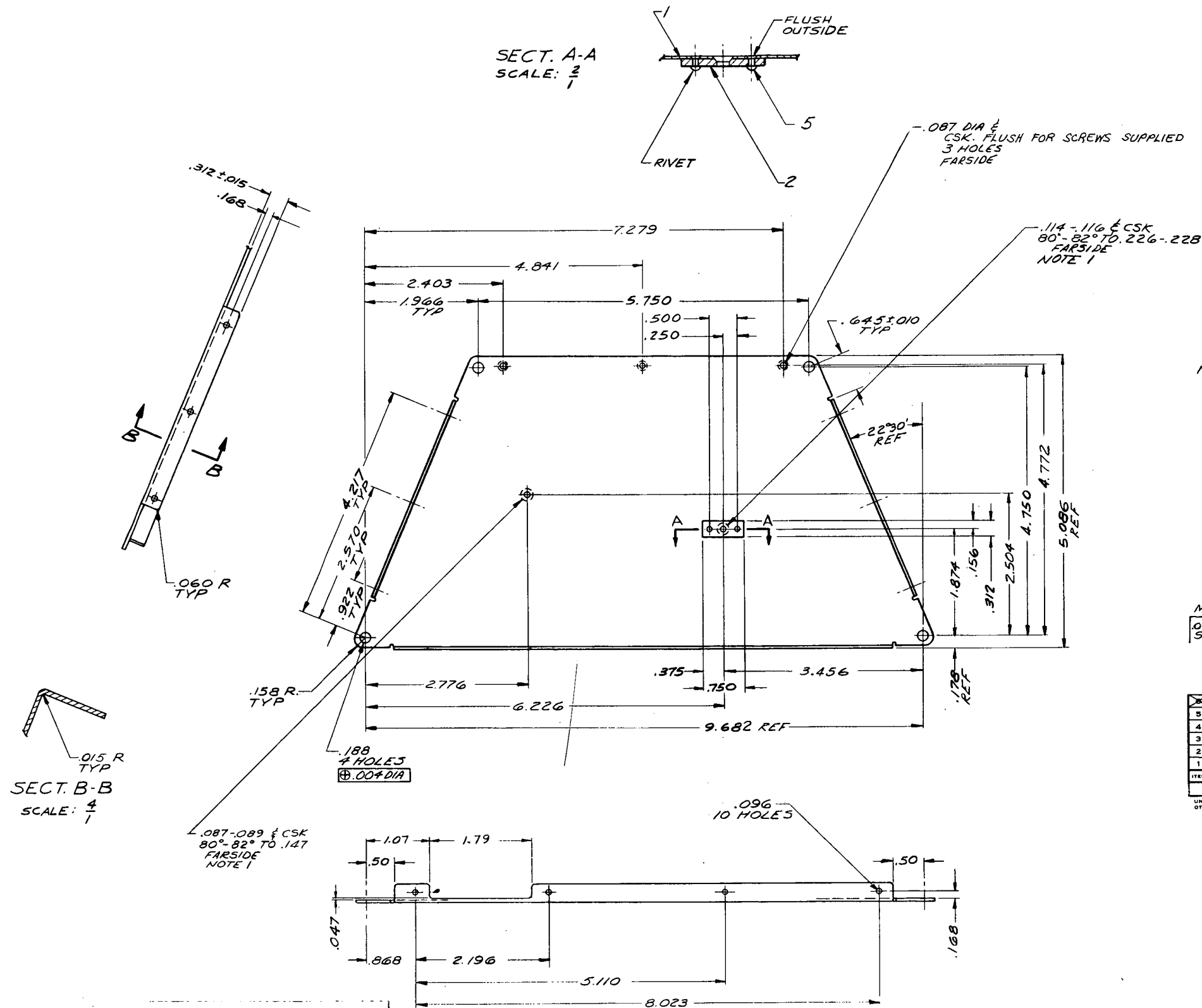
STOCK LIST

UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES. NONLIMITED DIMENSIONS
OTHER THAN SIZE OF RAW MATERIAL SHALL BE HELD AS FOLLOWS WHEN EXPRESSED:
TO 2 DECIMAL PLACES $\pm .02$ AS ANGLES \pm
TO 3 DECIMAL PLACES $\pm .003$

Figure 28. Top Cover Assembly

FOLDOUT FRAME #1
PRECEDING PAGE BLANK NOT FILMED

FOLDOUT FRAME #2



- NOTES:
1. THESE HOLES TO BE DRILLED BY B.T.L. AT ASSY.
 2. REMOVE BURRS & BREAK SHARP EDGES.
 3. ANODIZE IN ACCORDANCE WITH MIL-A-8625 TYPE II, DYE BLACK.

MATERIAL ITEM 1	MATERIAL ITEM 2
020 ALUMINUM SHEET 6061-T6	060 ALUMINUM SHEET 6061-T6

ITEM	PIECE	NAME	REQ
5	1	RIVET FLAT HD 100° CSK 1/16 DIA X .156 LG AL-2024	2
4	1		
3	1		
2	1	PLATE	1
1	1	COVER	1

STOCK LIST

UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES. UNLIMITED DIMENSIONS OTHER THAN SIZE OF RAW MATERIAL SHALL BE HELD AS FOLLOWS WHEN EXPRESSED:

TO 1 DECIMAL PLACES, .01/ AS ANGLES 2

TO 3 DECIMAL PLACES, .003

Preceding page blank
59.1

59.2

Figure 29. Bottom Cover Assembly

SECTION 3

COMPONENTS

3.1 Reliability and Screening

The IMP-F and -G experiments were designed and constructed for an operating lifetime of two years in space. To realize this goal, effort was directed toward a conservative design with functional redundancy, reliable components, quality construction, and frequent inspections.

Table 2 lists the types and quantities of components used in each experiment. With a total of 2414 components required to operate for two years, only high-reliability devices with failure rates on the order of 0.002 percent per 1000 hours could be considered. Bell Telephone Laboratories has acquired extensive experience with high-reliability components through programs such as Telstar and the submarine cable.

Only types of components which from past experience had proven consistently dependable were selected for this program. Most of these were ordered to BTL specifications. In addition, short-term, 100 percent screening tests were used to improve reliability by eliminating occasional early failures and unstable devices. Components which, during screening, showed changes greater than the median for the group, even though they may have still been within tolerance, were not used. The test conditions were carefully chosen to accelerate failure and drift of sub-normal components without impairing the life of normal ones.

Table 3 shows a list of the various screening specifications. For design applications, all manufacturers' ratings were derated at least 50 percent. Great care was exercised in handling and attaching the screened components to preserve their integrity.

Preceding page blank

TABLE 2. COMPONENTS USED IN BTL IMP-F AND -G EXPERIMENTS

<u>Component Type</u>	<u>Quantity per Experiment</u>
CAPACITORS	
Solid tantalum	149
General-purpose ceramic	124
Tubular ceramic	<u>51</u>
Total Capacitors	324
RESISTORS	
Carbon composition	438
Metal oxide film	26
Tantalum thin-film (integrated circuits)	<u>851</u>
Total Resistors	1315
TRANSISTORS	
NPN silicon	214
PNP silicon	247
PNP germanium	19
P channel FET	<u>4</u>
Total Transistors	484
DIODES	
Tunnel	22
Signal	<u>262</u>
Total Diodes	284
Transformers, Inductors, and Delay Lines	<u>7</u>
Total number of components:	2414

TABLE 3. SPECIFICATIONS AND SCREENING PROGRAMS

Type	Specification/Screening
CAPACITORS	
Solid Tantalum	<p>2.2-μF and 15-μF capacitors, with manufacturer's rated operating voltage of 35 volts, supplied by Kemet Department, Linde Company, division of the Union Carbide Corporation, under BTL Specification KS19458. All capacitors were given an additional screening at BTL as follows:</p> <ol style="list-style-type: none"> 1. Capacitance and equivalent series resistance measured at 150 Hz and 10 kHz, at room temperature. 2. Leakage measured at rated voltage and at 1.7 x rated voltage. 3. Temperature cycling, consisting of five cycles between +85°C and -60°C over a 24-hour period. 4. A 100-hour life test at +85°C under rated voltage. Capacitance and effective series-resistance measured at 150 Hz at room temperature. 5. Leakage measured at rated voltage. 6. Noise test consisting of a short-term leakage-variation measurement at rated voltage. <p>Rated voltage in the foregoing tests is the manufacturer's rating, derated to one-half for end use. Capacitors qualifying for flight use had a failure rate of less than 0.001% per 1000 hours.</p>
Ceramic	<ol style="list-style-type: none"> 1. General-purpose capacitors, from 10 pF to 10,000 pF, with a manufacturer's rated operating voltage of 200 volts, supplied by Vitramon, Incorporated; manufactured and tested in accordance with BTL specifications GA9910, G300104, and G300105. 2. Temperature-compensated tubular ceramic capacitors, 5 pF to 1000 pF, with a manufacturer's rated operating voltage of 500 volts, supplied by Erie Technological Products, Incorporated; manufactured and tested in accordance with BTL specification GA9910, Revision G, and Erie EP3210.

TABLE 3. SPECIFICATIONS AND SCREENING PROGRAMS (Continued)

Type	Specification/Screening
CAPACITORS (continued)	
Ceramic (continued)	<p>Both types of capacitors were screened at Bell Telephone Laboratories as follows:</p> <ol style="list-style-type: none"> 1. Capacitance and conductance measured at 1 kHz. 2. Life test for a minimum of 100 hours at room temperature under rated voltage. 3. Capacitance and conductance measured at 1 kHz. <p>Capacitors of these types qualifying for flight use had a failure rate of less than 0.002% per 1000 hours.</p>
RESISTORS	
Carbon Composition	<p>Type CD and EB resistors, supplied by the Allen Bradley Corporation.</p> <p>All resistors were screened at Bell Telephone Laboratories in groups taken from the same manufacturing lot for each value screened. The screening procedure was as follows:</p> <ol style="list-style-type: none"> 1. Resistance measured at room temperature. 2. Baked at +105°C for 96 hours. 3. Resistance measured at room temperature. 4. Ten temperature cycles between -55°C and +85°C for 120 hours. 5. Resistance measured at room temperature. 6. Noise level measured. 7. Baked at 105°C for 96 hours. 8. Resistance measured at room temperature. <p>Acceptability was based on any change in resistance occurring between step 3 and step 8 being within the norm for the group, and also on the noise level measured in step 6. Resistors qualifying for flight use had a failure rate of 0.0001% per 1000 hours or less.</p>

TABLE 3. SPECIFICATIONS AND SCREENING PROGRAMS (Continued)

Type	Specification/Screening
RESISTORS (continued)	
Metal Film	<p>Types NA60D and RN55D resistors were supplied by Corning Electronic Products Division.</p> <p>The screening procedure for metal-film resistors is identical to that given above for carbon-composition resistors.</p>
TRANSISTORS	
Silicon Bipolar	<p>Supplied by Motorola Semiconductor Products, Inc.; ordered to meet the requirements of MIL-F-19500 and G657490 in addition to BTL specifications G383745 for type 2N2222 and G383746 for type 2N3251. Types 2N2222 (NPN) and 2N3251 (PNP) were chosen on the basis of their suitable electrical characteristics, reliability demonstrated through use in other BTL programs, and good tolerance to radiation damage (on the basis of several sample lots tested). (Prior experience had shown Motorola capable of delivering devices to these specifications. However, because of the short program schedule and unexpected difficulties encountered, many devices were accepted without meeting the full specifications.)</p> <p>Screening was done by the manufacturer on a lot basis. A prior condition for lot acceptance was a sample radiation test. All transistors in lots meeting this requirement were then subjected to the following preconditioning steps, in the order listed:</p> <ol style="list-style-type: none"> 1. Temperature aging at +250°C for 60 hours. 2. Temperature reverse voltage at +175°C for 100 hours (PNP devices only). 3. Life defect according to G657491, Method I, 3X rated power at +25°C for two hours. 4. Temperature cycling to MIL-FTD750, Method 1051, Condition C. 5. Constant acceleration at 20,000G. 6. Shock 5 blows to MIL-FTD750, Method 2016. 7. Particle test to G657491, Method 201.

TABLE 3. SPECIFICATIONS AND SCREENING PROGRAMS (Continued)

Type	Specification/Screening
TRANSISTORS (continued)	
Silicon Bipolar (continued)	<p>8. Leak test at 90 lbf/in² for 1 hour.</p> <p>9. Leak test at +180°C to G657491, Method 6.</p> <p>A five-parameter electrical test was performed on each device following steps 1, 2, 3, 5, and 6. For lot acceptance, a PDA (percent defective allowed) of 15% applied to each step except 1, 4, and 5. In these steps, defectives were removed before proceeding. A total PDA of 30% applied for all steps following 1. All transistors in accepted lots were given a visual and mechanical examination and an electrical test which measured 16 parameters. A sample group of devices was subjected to additional environmental and mechanical tests, some of which were destructive. The supplier was unable to meet lot pre-conditioning requirements for the 2N3251; these devices were supplied, instead, to an expanded version of MIL-F-19500 (plus sample radiation tests). The radiation tests had to be waived for most of the 2N2222 devices; for some lots, a MIL specification was substituted for preconditioning to expedite delivery in time to meet the schedule. Those transistors for circuit applications where radiation damage was critical were screened and selected at BTL.</p>
Germanium Transistors	2N964A (PNP) transistors for a special application in thin-film discriminators, also supplied by Motorola; ordered tested to BTL specification G365393.
Field-Effect Transistor, Unipolar, "P" Channel	2N2608 (FET) transistors were used in the multiplier circuit; supplied by Siliconix, Incorporated, meeting requirements of BTL specification G365394.
DIODES	
Tunnel Diodes	<p>1N3713 germanium tunnel diodes, supplied by the General Electric Corporation. The screening of these devices was performed at Bell Telephone Laboratories as follows:</p> <ol style="list-style-type: none"> 1. Shock 5 blows 1500G per MIL-STD750, Method 2016. 2. Constant acceleration 20,000G, 1 minute, per MIL-FTD750, Method 2006.

TABLE 3. SPECIFICATIONS AND SCREENING PROGRAMS (Continued)

Type	Specification/Screening
DIODES (continued)	
Tunnel Diodes (continued)	<ol style="list-style-type: none"> 3. Vibration variable frequency, 100-2 kHz, per MIL-FTD750, Method 2056. 4. Mechanical inspection. 5. Electrical measurement of 4 parameters. 6. Life defect (high-temperature accelerated aging test). All units were subjected to 250 hours at +100°C under bias. Dc tests were made at 24 hours, 100 hours, and 250 hours during this step. 7. Electrical measurement of 4 parameters at room temperature. <p>The above tests were designed to assure 0.001% per 1000 hour failure rate at 50°C, based on previous experiments done on diodes of the same type.</p>
Signal Diodes	High-reliability silicon epitaxial signal diodes, supplied by the Western Electric Company; manufactured and screened to specification GA53930; electrically tested to GF-40163-L1-3.
TRANSFORMERS, INDUCTORS, AND DELAY LINES	
<p>These devices were specially made by the Components Laboratory of Bell Telephone Laboratories, Whippany, New Jersey. The following types of devices were supplied.</p> <ol style="list-style-type: none"> 1. Modified M-derived five-section delay line. 2. Five-winding noise-rejection transformer. 3. Bias-supply oscillator transformer. 	

3.2 Thin-Film Integrated Circuits

Bell Telephone Laboratories, in collaboration with the Western Electric Company, designed, developed, and produced the thin-film integrated circuits for the IMP-F and -G experiments.⁶

The first step in producing these integrated circuits was to determine the most efficient layout. The thin-film resistors required so little area that the main factor determining substrate size was adequate clearances between the discrete components. A standard width of 0.63 inch was adopted for the three active circuits (A, B, and C in Figure 6); this allowed room for two parallel rows of transistors with tantalum capacitors mounted between the rows, as seen in Figure 7. Components were arranged to produce a circuit pattern with minimum crossovers and with adequate areas for resistors. Unavoidable crossovers were made with wire straps on the component side. The thin-film resistor layouts fitted easily into the available areas using line widths well within the state of the art. The narrowest line width used was 3 mils, for the two 56K-ohm resistors shown just above center on the amplifier substrate in Figure 7. Low-value resistors were made wide to increase their track length and thereby minimize the effects of variations in screening on the electrolyte solution prior to anodization.

Each type of circuit was batch processed, 15 or more at a time, on a 3-3/4 x 4-1/2 inch master ceramic substrate which was later sliced into individual circuits with a diamond saw. The substrate material was 0.030-inch-thick, high-density aluminum oxide ceramic (alumina). Lead-hole patterns were punched in the alumina while it was in the green state (unfired). After firing and glazing, the master was sputtered with a uniform film of tantalum nitride having a sheet resistivity of 50 to 60 ohms per square. Several successive layers of thin metal films for the conductors and terminations were evaporated onto the substrate, starting with nichrome, then copper, then palladium on the outer surface. The groups of conductor patterns were then photoetched on the metal films. Next, the resistor tracks were formed by etching the exposed tantalum between the conductors. Each resistor on the master substrate was adjusted individually to final value by anodizing its surface. This process converted the surface of the tantalum electrolytically to an insulating layer of tantalum pentoxide; the depth of anodization determined the final resistance. Since resistance could only be raised by this process, all resistors on the substrate were initially made 20 percent lower than the design value. The anodizing process was automatically controlled by a bridge circuit which monitored the resistance and shut off the current when the preset value was reached. Resistance tolerances of 1 to 5 percent were specified for these circuits, although the process was capable of

far greater accuracy. Tantalum film resistors, protected by their inert covering, were unaffected by normal handling during component-assembly operations. Although the same fabrication process used for resistors was available for tantalum film capacitors, their larger area requirements and limited capacity range made this application unsuitable. Instead, discrete ceramic and solid tantalum capacitors were applied to the circuit with the transistors and diodes.

After the master substrate was sliced into individual circuits, each circuit substrate passing all in-process inspections was assembled with its components, straps, and terminal leads. Soldering was accomplished by flux-coating the thin-film circuit side of each substrate and immersing it in a solder pot for several seconds. Following cleaning and final visual inspection, the completed integrated circuits were shipped to the BTL Murray Hill laboratory. No electrical tests other than resistance measurements on the unassembled substrates were performed at the assembly laboratory (Allentown, Pennsylvania).

Before final testing, all thin-film integrated circuits were given a follow-up inspection and were assigned serial numbers and inspection cards. Electrical tests were performed on a multicircuit test stand⁷ which could accommodate half the total complement of circuits for one experiment. The test stand was designed to fit into a temperature chamber and connect to a remote test panel through a multiple feed-through connector interface. Power supply lines, inputs, and outputs of all circuits under test could be examined through selection by a system of switches.

Operational checks and reference measurements of critical parameters were first made at room temperature and recorded on the inspection card. Particular emphasis was placed on pulse characteristics, which were examined by oscilloscope. Following these tests at room temperature, the circuits were temperature-cycled between +60°C and -20°C (exceeding the experiment test specification by 10°C in each direction). The test continued for five complete cycles of 1-hour duration each. After this, the high and low temperature limits were sustained and the initial test sequence was repeated. A last test sequence was performed at room temperature, for comparison with the first sequence to verify stability. All units completing the test were visually inspected for any change in appearance resulting from temperature cycling. The recorded temperature performance data for each circuit was then carefully examined. Any units showing abnormal tendencies were rejected for flight use.

Omega-shaped strain-relief bends were formed in all terminal leads with a special multiple-lead bending tool before the component side of each substrate was

encapsulated as described in paragraph 4.4.1. These bends were essential to prevent strains on the substrate, since the encapsulated units were mounted directly against the printed circuit boards.

Each experiment required the following quantities of the five types of integrated circuits used:

- (a) 24 operational amplifiers;
- (b) 19 zero-crossing discriminators;
- (c) 8 pulse shapers;
- (d) 40 linear gates;
- (e) 36 potentiometer networks.

SECTION 4

CONSTRUCTION

4.1 Printed Circuit Boards

4.1.1 Art Work. - The printed-circuit art work was produced by applying black tape to a Mylar overlay on the twice-size layout drawings described in paragraph 2.3.1. Printed path width was typically 0.032 inch, with a minimum of 0.020 inch in special situations. The same dimensions applied to the clearance between paths. Solder lands were the elongated circular type in various sizes, depending upon layout requirements but always providing a minimum length of 0.08 inch clinched lead contact. Terminal lands at the ends of the boards were designed to mate with commercial printed-circuit board connectors on the system test stand and then later to serve as soldering lands for the interconnecting harness wires.

Clearance holes in the copper for component leads were provided on the ground-plane side of the board. The art work for this was prepared using a reversed print of the layout. A pattern of lands for the ground-plane through-connections, to be selectively solder-plated on the copper, was also produced from this print. Registry between all three pieces of art work was aided by punched targets on each print referenced to the centers of the through-bolt holes shown on the layout.

4.1.2 Fabrication. - All printed circuit boards were processed at Bell Telephone Laboratories, Murray Hill, New Jersey. For the most part, standard printed-circuit techniques were applied. The board material was 0.040-inch-thick Fiberglas-epoxy with 1-ounce copper on both sides. Separate oversized blanks were cut for each circuit board to be processed and were predrilled with the hole pattern shown in Figure 22. A drill jig was used to assure accurate and repeatable hole spacing. This was important for proper alignment of the three printed-circuit patterns and the accuracy of the in-process machining to follow. Circuit boards were protected during machining by cardboard separators and inspected for scratches or other damage after each operation before the next step in the sequence was begun.

Half-size negatives of the art work were accurately punched with 0.114-inch-diameter holes centered on two of the circuit-board holes used as reference targets. A frame, consisting of two lucite plates with the same hole pattern and fitted with short dowel pins, was used to hold the negatives in alignment on both sides of the photosensitized circuit-board blank during the exposure process.

After the circuit pattern was etched, the blanks were carefully milled to the correct width. Electroless copper was then deposited on the milled edges, overlapping the ground plane by 0.05 inch for electrical contact. These edges and the terminals at the end of the board were gold plated to maintain good conductivity. The printed circuit and the ground-plane lands were solder-plated; the remainder of the ground plane was not solder-plated in order to conserve circuit-board weight. After completion of the printed-circuit process, the ends of the boards were milled to their final lengths and all component lead holes were drilled. Each circuit board was thoroughly inspected for defects or damage, as described in paragraph 4.3.5, before being accepted for flight use.

4.1.3 Preparation for Assembly. - Before components were mounted on the printed circuit boards, the following preparations were made:

- (1) Strap wires were installed and soldered between the ground plane on one side of the board and grounded portions of the printed circuit on the other side.
- (2) The ground plane was insulated with a 1-mil-thick thermal-adhesive coated Mylar sheet applied under heat and pressure. This material produced an excellent bond to the board, following even the contour of the etched pattern in the 1.5-mil-thick copper.
- (3) The Mylar insulation was trimmed along the edges and all holes for component leads were pierced.

4.2 Assembly Area

Figure 30 shows the IMP-F and -G experiments flight-hardware assembly room. "White room" conditions were not required for this project. The main objective was to provide a controlled area, separate from other less critical laboratory operations, where flight hardware could be safely assembled and stored. Assemblers wore white nylon coats to prevent possible contamination from metallic particles which might have been picked up on their street clothing while elsewhere within the building. Smoking and eating were prohibited in this area, and only authorized personnel were admitted. The room was air-conditioned by an internal unit; a separate, filtered fresh-air system provided a slight positive pressure. A laminar-flow hood was in continuous operation to reduce the overall dust level and provide a local white working area when occasionally needed. Isolation between individual work positions was achieved through the use of plastic bench-top enclosures, shown in Figure 30. These enclosures were fully open at the front and wide enough not to restrict movements of the assemblers. In this way, wire lead clippings and bits of

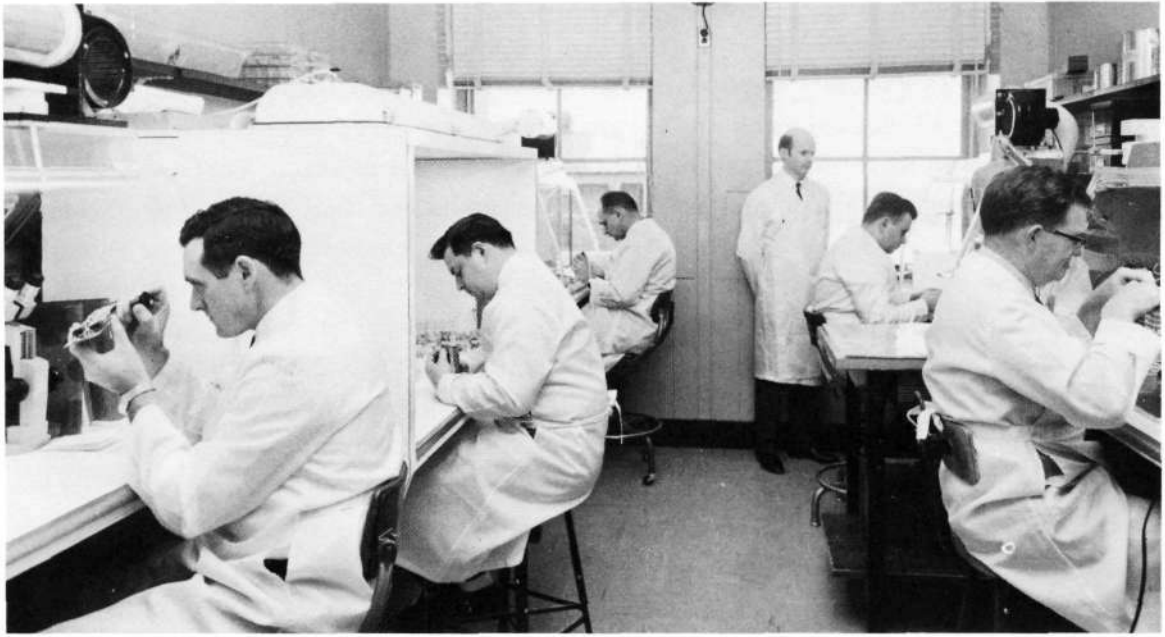


Figure 30. IMP-F and -G Experiments, Flight-Hardware Assembly Room

solder were limited to each work location, where they were easier to control. Visibility of these scraps was increased by using replaceable white cardboard on the work surfaces. The enclosures also kept other items not essential to a particular assembly operation from cluttering the work positions and protected the work from damage should anything fall from overhead storage shelves. All flight parts and subassemblies in process were kept in plastic containers and transferred from the work benches to a locked storage cabinet at the end of the day. Polyurethane foam encapsulation of all completed hardware was performed under an exhaust hood located in one corner of the room.

The assembly staff consisted of four assemblers (one of whom was the lead man and inspector), a technician, and a packaging manager. Two assemblers spent their full time mounting and soldering components to printed-circuit motherboards. A third specialized in the interconnecting harness wiring. The lead man/inspector managed the work assignments and bookkeeping, performed special preparatory operations on the printed circuit boards before assembly, and inspected all work at prescribed milestones. The technician's responsibility was component procurement, stock control, integrated-circuit screening, and the assembly parts kits. The packaging manager was responsible for all phases of the assembly program and for quality control.

4.3 Motherboard Assembly

4.3.1 Parts Kits and Records. — All parts, parts lists, special instructions, and inspection sheets for each motherboard were prepared in kit form in advance of assembly and were stored in plastic containers until needed. Parts kits were prepared in display form by inserting the components upright into a sheet of styrofoam, as shown in Figure 31. This arrangement was convenient and speeded assembly time by reducing the amount of searching and handling otherwise necessary if parts had been supplied in envelopes. A parts list with each kit identified all components by circuit number, value, tolerance, and type. An inspection sheet for recording information concerning the status of the motherboard was attached to the front of the parts list. Headings and spaces on this sheet were provided for each construction milestone and were to be dated and initialed by the assembler and inspector upon completion. Each printed circuit board was stamped with a serial number which identified it with its assigned paper work. One of the duties of the inspector was to maintain a chart showing the status of all motherboards being processed. At the beginning of the project, a list of general assembly practices and handling procedures was issued to all assemblers. Instructions for special operations on each type of board were included with the kit paper work.

Master assembly drawings for each board contained all the information necessary to identify and place the components and strap wiring. No other copies were used, and the masters were updated as changes were made.

4.3.2 Assembly Practices. - Assembling carefully screened components onto the motherboards without degrading their reliability called for special handling precautions.

Figure 32 shows a motherboard being assembled while clamped in a handling fixture. Grooves milled in the frame of this fixture held the board by its edges to prevent warping during component mounting and soldering operations. The fixture could be rotated axially for rapid access to either side of the board. In this way, the motherboards were placed in an ideal working position for the assembler and were protected against dropping. Mounted components were kept out of contact with the work-bench surface where they might be damaged or pick up lead clippings and solder scraps.

Component leads were bent by using specially contoured pliers to isolate bending forces from the component body and to prevent marking the leads. Lead bends had a minimum radius equal to twice the lead diameter and were not closer than

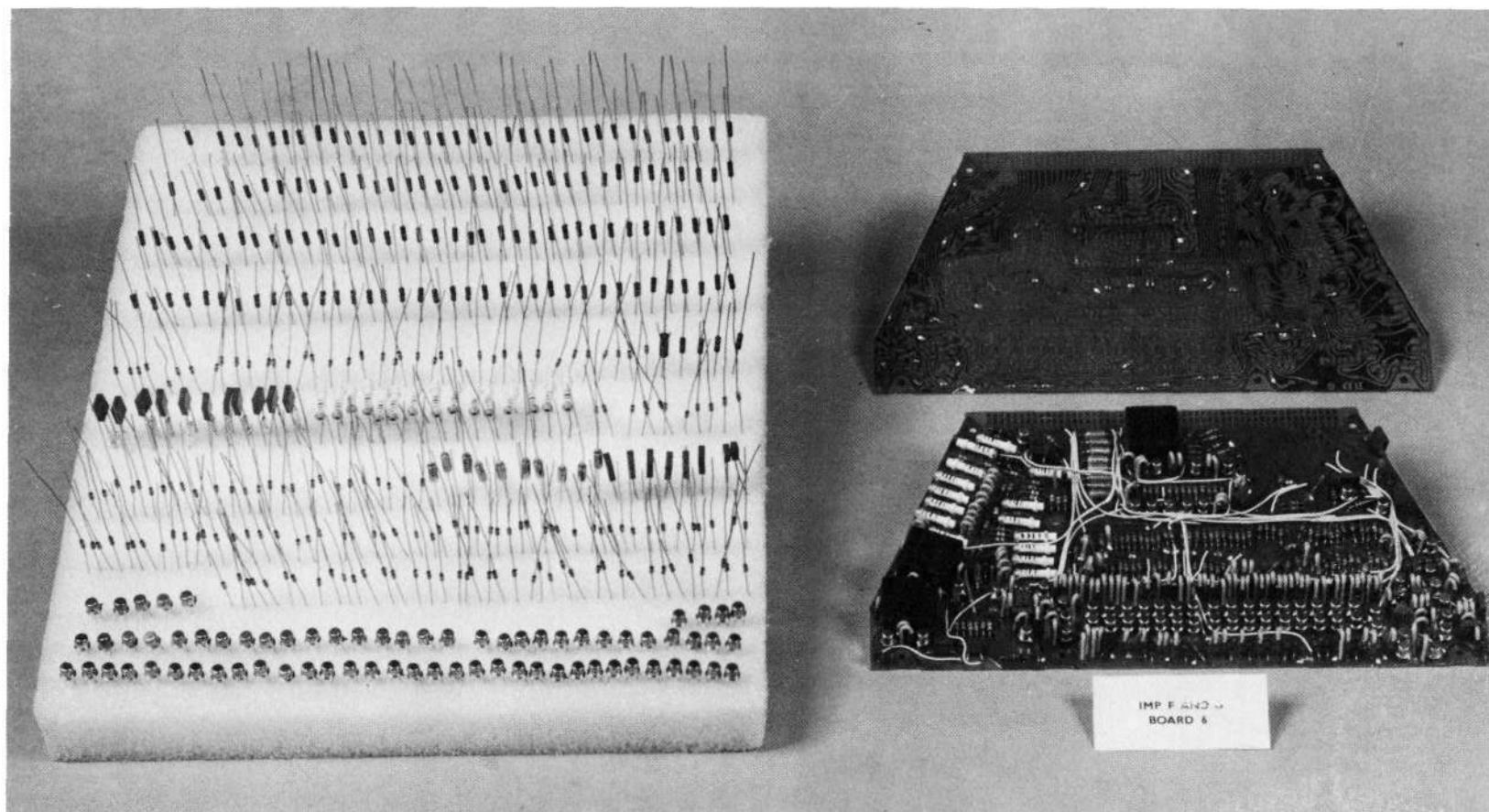


Figure 31. Parts Kit and Completed Board for Motherboard 6



Figure 32. Assembly of Motherboard 6

1/16 inch to the component body or end seal. Mechanical shock from lead clipping was isolated from the component body with pliers clamped between it and the cutting point. Axial lead components were, in general, mounted horizontally against the board. However, in a few areas of unusually high density, resistors and diodes were placed vertically. In these situations, the lower end of the component was spaced 0.05 inch from the board. Ceramic capacitors with end radial leads were spaced 0.1 inch from the board to permit the attachment of heat-sink clips during the soldering operation. Transistors were raised by the same amount to avoid stressing the header seals during lead clinching. Special spacing gages were provided for each type of component to speed the mounting process. Assemblers were instructed never to twist or pull on component leads during the bending or mounting operations; such stresses could break the seal between the lead and component body. In certain dense vertical-mounting situations, leads were jacketed with a silicone-varnished Fiberglas sleeving as a protection against shorting to one another during the encapsulation process. Strap wiring was insulated No. 24 solid tinned copper wire; its insulation was thermally stripped to prevent nicking the conductor. Component leads and straps were clinched against their respective printed-circuit lands and cut to a length of 0.08 inch from the mounting hole. No soldering was done until all components and wires were mounted and their correct values and placements were verified by the inspector.

4.3.3 Soldering. - Weller Electric Corporation model W-TCP temperature-controlled soldering irons, equipped with 700°F, 1/16-inch, screwdriver-type, replaceable tips, were used exclusively. These irons were small, lightweight, and ideally suited to printed-circuit board work. A wet sponge in a holder was provided for frequent cleaning of the iron-clad tips, to assure optimum heat transfer to each connection. The solder for most applications was 0.025-inch-diameter Kester 60/40 with a pure rosin-flux core.

Components with soft solder seals or internal connections (i.e., tantalum and ceramic capacitors) were protected from damage during soldering by small, flat jaw, copper heat sink clips attached to their leads. Trimming components were temporarily mounted and tack-soldered with unclinched leads for easier removal after testing.

A rapid and effective vacuum-operated desoldering device was devised for removing solder from unsatisfactory joints. It consisted of a large, thick-walled glass-flask reservoir connected to a half-atmosphere house vacuum line. A glass medicine dropper was fitted to a rubber hose which, in turn, was attached to glass tubing extending through a rubber stopper to the bottom of the flask. Water at the

bottom of the flask trapped and prevented solder particles from entering the vacuum line. The shape of the dropper nozzle produced a high-velocity inward air flow which removed solder from a heated connection so efficiently that, in most cases, the lead became free. Most important, the whole operation could be performed so rapidly that no heat damage to the printed circuit boards occurred. Several commercial desoldering devices had been tried; all proved ineffective and, in some cases, detrimental to the printed circuit board. Only the assemblers were permitted to solder or desolder components. This prevented degradation of connections and components from tack-soldering by technicians during the testing and trimming operations. Although all soldering flux used was inert, it was nevertheless cleansed from the boards after assembly to facilitate inspection of the solder joints and prevent adherence of foreign particles.

4.3.4 Testing and Trimming. - As mentioned in paragraph 4.1.1, the circuit boards were designed to plug into printed-circuit connectors on a large system test stand. The test stand was designed to simulate as nearly as possible the configuration of the electronic stack in its assembled form, to obviate further adjustments after final assembly. Each board could be separated from the rest of the stack while still electrically connected, permitting access to all test points on both sides of the board, or it could be quickly disconnected from the test stand for adjustment of component values and then reinserted to continue the test. The test stand provided security and stability for the boards on the bench; it was also designed for operation within a Wiley model C-106-3600 temperature chamber. The usual hazards associated with testing a temporarily connected system of unencapsulated boards were therefore greatly reduced.

Trimming an experiment of this complexity involves the careful adjustment of many interacting parameters such as amplifier gains, discriminator levels, pulse shapes, and timing. Many of these adjustments were made with miniature, wire-wound, trimming potentiometers. However, no mechanically variable components were considered reliable enough for space applications. As the adjustments for each section of the experiment were completed, the potentiometers were removed from the circuit boards without disturbing their settings and carefully measured on a resistance bridge. A thin-film potentiometer network consisting of a set of binary weighted resistors, shown in Figure 6(D), was used to replace each variable component. These resistors could be set within 1 percent of full scale by shunting elements of the resistor string with solder across narrow gaps in the conductor pattern. The whole operation was performed with the aid of a microscope by an assembler specially trained in the intricacies of soldering to the small, plated circuit paths on the ceramic substrates. Although the gap to be spanned was only 5 mils wide, for

a reliable connection it was necessary to install a mechanical bridge in the form of a hot, solder-coated, No. 36 copper wire before applying solder. Liquid flux was used to assure an even and rapid wetting of the plated paths. The potentiometer networks could be adjusted at the rate of approximately 12 per hour. Previously adjusted networks could be changed by carefully cutting out a section of the fine wire bridge, with the aid of a microscope, using a small knife blade. After a check of resistance setting, each thin-film resistor network was permanently installed in its respective trimming potentiometer location on the circuit board. The board was returned to the test stand to recheck the levels for agreement with the previous adjustments.

In the case of capacitors, adjustable elements were removed from the boards, measured, and substituted with fixed, temperature-compensated, ceramic capacitors of the nearest commercially available value. The small differences sometimes occurring between the fixed and variable elements were compensated by adjustment of trimming resistors elsewhere in the circuit.

4.3.5 Inspection. - Thorough inspections were performed at various milestones in the sequence of assembly operations, beginning with the printed-circuit board blanks and continuing through completion of the experiment package. The inspector was highly skilled in his field, having served in the same capacity during the fabrication of electronic assemblies for the Telstar program. A wide-field binocular microscope with an adjustable range of magnification from 7X to 80X aided in the close examination of components and connections. Table 4 outlines the test procedures and sequence.

TABLE 4. INSPECTION PROCEDURES AND SEQUENCE

<u>Area</u>	<u>Operation</u>
Printed Circuit Boards	<ol style="list-style-type: none"> 1. Inspect predrilled blanks for flaws and scratches in the copper surface before delivery to the printed-circuit shop. 2. Inspect the boards after machining to specified width, prior to edge plating, for damage to the circuit pattern, roughness of the milled edges, and correct width of the board. 3. Inspect each board after completion of all printed-circuit processing, final machining, and hole-drilling operations for the following: <ol style="list-style-type: none"> (a) Scratches on <ol style="list-style-type: none"> (1) paths and lands extending through solder plating and into copper; (2) the surface of the substrate bridging paths or lands. (b) Holes and notches in the paths resulting from the printed-circuit process (these must not exceed 25 percent of the path width). (c) Lifting of printed paths and lands. (d) Uniformity of solder-plating. (e) Metallic bridging between paths and lands. (f) The condition of the over-edge plating: <ol style="list-style-type: none"> (1) clearance to conductors on the printed-circuit side (0.020 inch minimum); (2) smoothness and uniformity. (g) Dimensional accuracy. (h) General condition of the board: <ol style="list-style-type: none"> (1) sharpness of the printed circuit pattern; (2) clearance areas in the ground plane; (3) errors or omissions in the drilling of the component mounting holes; (4) cleanliness. 4. After mounting and soldering the strap-wire through connections between the ground plane and printed circuit,

TABLE 4. INSPECTION PROCEDURES AND SEQUENCE (Continued)

<u>Area</u>	<u>Operation</u>
Printed Circuit Boards (continued)	inspect them for the quality of the soldered connections and any strap omissions.
	5. Inspect each board after completion of the Mylar-insulation bonding process for a proper bond and general appearance.
Components and Integrated Circuits	Visually inspect all parts prior to preparing the assembly kits.
Partially Assembled Motherboards, Mounted Components	<p>Inspect the partially assembled motherboards (all components excluding thin-film circuits mounted but not soldered).</p> <ol style="list-style-type: none"> 1. Inspect for correct assembly. Verify components with the assembly drawing and parts list as follows: <ol style="list-style-type: none"> (a) Type of component. (b) Value of component. (c) Polarity. (d) Location of component. 2. Inspect the mechanical condition of components and board for the following: <ol style="list-style-type: none"> (a) Correct positioning and clearance of components and leads. (b) Lead bends. (c) Any damage to components, their leads, or the printed circuit due to mounting operations.
Strap Wiring	<p>Inspect after all components have been soldered and strap wiring has been installed but not soldered.</p> <ol style="list-style-type: none"> 1. Verify the correct connection, routing, and dress of each strap wire with the assembly drawing. 2. Check for possible damage to the components, strap wire, insulation, and printed-circuit pattern as a result of installing the strap wires.
Completely Assembled Motherboards	Inspect the completely assembled motherboard following mounting of the thin-film circuits and soldering of all remaining connections as follows:

TABLE 4. INSPECTION PROCEDURES AND SEQUENCE (Continued)

<u>Area</u>	<u>Operation</u>
Completely Assembled Motherboards (continued)	<ol style="list-style-type: none"> 1. Check the condition and appearance of all components and leads. 2. Check for wire clippings, solder balls, and other foreign particles which may have become entrapped among the components or printed circuit. 3. Inspect all solder connections for compliance with established acceptance standards.
Tested and Trimmed Motherboards	<p>Inspect all motherboards after testing and trimming, following the installation of fixed components in place of adjustable ones.</p> <ol style="list-style-type: none"> 1. Check for correct placement and value of replaced components and the quality of their solder connections. 2. Look for damage resulting from the testing and trimming operations. 3. Make a final search for entrapped foreign particles on both sides of the board. Perform a general vacuum-cleaning operation using the same type of device described for desoldering.
Encapsulated Motherboards	<p>Inspect each motherboard after the foam-encapsulation process for the following:</p> <ol style="list-style-type: none"> 1. The condition of the foam encapsulation. <ol style="list-style-type: none"> (a) Uniformity and density; (b) Dimensions; (c) Cavities exposing components or leads. 2. Damage to the printed circuit from handling during the process. <p>Sign off boards which have passed this final examination on the inspection sheet. File all signed inspection sheets, notes, and parts lists for each board in the applicable flight-model notebook.</p>
Interconnecting Harness Wiring	<p>Inspection is described in Paragraph 4.5.2.</p>
Harness Encapsulation	<p>Disassemble housing. Inspect harness and other areas encapsulated with silicone rubber foam.</p>

4.4. Encapsulation

As described in paragraph 2.4.1, the component side of each motherboard was individually encapsulated in polyurethane foam. The material used was Emerson and Cumming, Inc. Eccofoam FP resin with catalyst 12-2. This mixture expands and cures to a semirigid, thermosetting, unicellular foam with a density of 2 pounds per cubic foot. Unlike its hard-setting counterpart, Eccofoam FPH, FP foam has some degree of flexibility and can be compressed without crumbling. This desirable property plays an important roll in the mechanical integrity of the assembled stack.

4.4.1 Integrated Circuit Encapsulation. - The thin-film circuits were mounted inverted on each motherboard, with their components sandwiched between the board and the ceramic substrate. To insure proper encapsulation, the components and substrates were prepotted prior to motherboard assembly. Figure 33 shows a nest of special molds used to cast the foam around the components. The thin-film substrates were inserted into flexible Silastic molds which were grooved near the bottom to hold the substrate edges. Teflon cover plates provided a nonadhering top

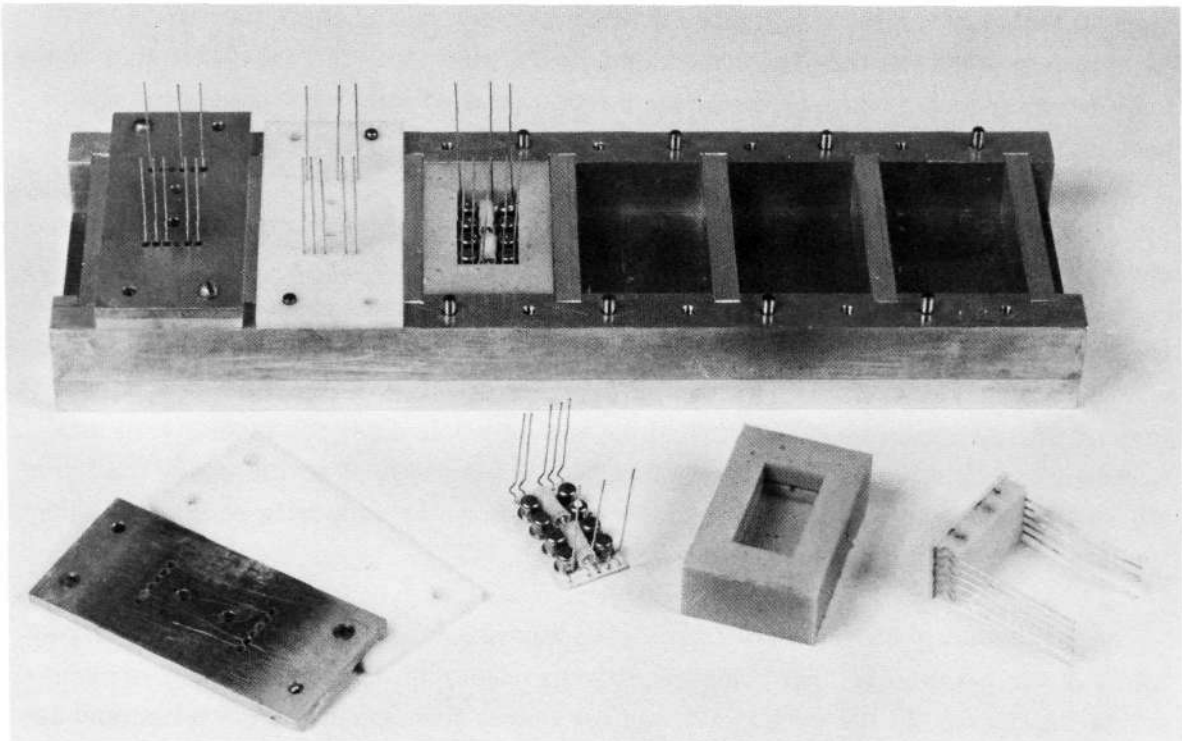


Figure 33. Foaming Molds for Integrated Circuits

surface for each mold; these were clamped under aluminum plates screwed to the side rails of the mold nest. Foam run-up on the terminal leads was prevented by inserting the leads through close-fitting holes in the Teflon plate.

When all molds and nests had been loaded, a small quantity of foam resin and the specified proportion of catalyst were placed in a disposable container and thoroughly blended with a spatula for 1 minute. The mixture was then quickly transferred to a 5-cc plastic syringe, and a small quantity was injected into each mold in the nest. A pair of concentric relief holes in the covers vented the mold as the foam expanded and also limited the generation of internal pressure. Full expansion of the foam took 5 minutes. Curing was accomplished in 1 hour at +60°C in a circulating-air oven. An encapsulated substrate is shown in the lower right corner of Figure 33.

4.4.2 Motherboard Encapsulation. - A procedure similar to the one described above was used to encapsulate the completed motherboards. Large Silastic molds were prepared for each type of motherboard. The molds were designed to hold the boards at the required depth in a snug-fitting groove around the inner edge of the mold. The mold was made slightly smaller than the board in order to keep the foam away from the edges so it would not interfere with the function of the finger-contact sheets at final assembly. A greater overlap was necessary along the rear edge of the board to mask the terminal area during encapsulation. Special clearances in the foam peculiar to a certain type of board were provided either by protuberances cast into the Silastic mold or by separate inserts.

The mold nest comprised an aluminum baseplate, a frame, and a thick plastic cover. The motherboard was accurately positioned within the nest by close-fitting dowel pins inserted into the two central through-bolt holes and then into corresponding holes drilled in the baseplate and cover of the nest. Aluminum sleeves, coated with a silicone release agent, were slid over the dowel pins above the board. These formed clearances in the foam around the through-bolt holes for insertion of the aluminum stack spacers at final assembly. The plastic nest cover sealed the top of the Silastic mold around the edges and was held down by wing nuts on bolts passing through holes around its perimeter.

Approximately 30 grams of foam resin was mixed with its catalyst and poured into a 30-cc plastic syringe. This quantity was much more than required to encapsulate the board, but the excess allowed for losses throughout the operation and assured enough foaming pressure within the mold to fill all voids. With the mold cover off, the mixed foam resin was injected onto the board; particular attention

was given to areas of greater impedance to foam flow. This operation was easily performed before installing the cover because the foam did not expand rapidly enough to fill the depth of the mold for several minutes after injection. With the cover in place, the progress of the expanding foam was observed through the plastic cover. Deficiencies could be corrected by injecting more foam through the cover venting holes. After the foam had expanded fully, it was cured by placing the mold in a circulating-air oven at +60°C for 1 hour.

4.4.3 Foam Planing. - The foam was molded deeper than necessary so that it could be accurately planed to its final height. This operation was performed in a fixture equipped with long, notched Teflon blocks which clamped and supported the boards along their front and rear edges. These blocks extended above the board to the desired height of the finished foam. Screws into threaded stand-offs under the central through-bolt holes held the board in place and supported it in the center. The planing operation was begun by first sawing off the excess foam somewhat above the Teflon blocks in order to remove the hard skin which forms on the top of molded foam. A very large, coarse, flat file was found to be best for planing because it cut with less applied pressure than a fine one and produced nearly identical results. The whole operation was performed gently and evenly until further cutting by the file was limited by the tops of the Teflon blocks. The finished foam surface obtained was moderately coarse, compressible, and level to within 0.010 inch of the design height.

4.4.4 Special Operations. - An electrostatic shield was molded into the foam above the components on motherboard 2. The stack was designed with greater spacing between boards 1 and 2 to maintain adequate printed-circuit-to-shield clearance. In a two-step operation, a gold-plated sheet of 1-mil-thick aluminum foil was bonded to the planed foam surface of motherboard 2. The board was returned to the mold and additional foam was cast above the shield. A second planing operation adjusted the thickness of the foam layer over the shield to 0.15 inch.

An 0.2-inch-thick self-supporting foam sheet was inserted in the stack between motherboards 4 and 5, where the two printed circuits faced each other (described in paragraph 2.4). This piece was made by first casting and planing a normal layer of foam on a blank circuit board. The top foam surface was then stuck to an aluminum plate with double-sided masking tape, inverted, and remounted in the planing jig. The blank board was cut off and the remaining foam on the aluminum plate was filed to the prescribed thickness.

After all the motherboards had been foamed and planed as described, they were mounted together in the correct sequence in a stack between two heavy aluminum plates. The whole stack was then pressed together to seat the solder-joint protrusions on the unfoamed, printed-circuit side of each board into the foam on the next board, to achieve a board-to-foam contact throughout the stack. Pressure was supplied for this operation by tightening large wing nuts on long bolts running through the stack and the aluminum plates. Before proceeding with the harness wiring, the stack of boards was assembled within the experiment housing to check for proper fit.

Two remaining foaming operations involving the harness wiring are described in paragraph 4.6.

4.5 Electronic Stack Assembly

4.5.1 Preparations. - After an inspection of all the encapsulated motherboards, the entire complement was ready for permanent interconnection as a flight electronic system. Dual-purpose terminal lands along the rear edges of the motherboards, which provided plug-in connection to the test stand during testing, now served as soldering lands for attaching the harness wires. The harness comprised 160 wires, with as many as 68 connections on a single board.

Wiring of the harness was done with the boards mounted on a simple jig consisting of an aluminum bar in which two long rods were anchored and spaced so that they could be inserted into the two inboard through-bolt holes on each motherboard. The jig was clamped in a small wiring vise equipped with a universal joint which permitted the harness work to be conveniently positioned. The assembler referred to enlarged prints of the terminal-land layouts and connection charts listing the terminal number, color code, origin, and destination of every wire for each board in the stack.

Raychem Corporation, specification 44, stranded No. 26 Outer Space Wire was used in the harness. Only white insulation was readily available and, since a large number of identifying color combinations were needed, coding was done by applying dots of colored paint to the end of the insulation as each wire was attached.

Before starting the harnessing operation, the gold plating was removed from all terminal lands to prevent embrittlement problems due to excessive gold concentration in the solder joints. Since gold dissolves rapidly in molten solder, removal was accomplished by wetting each terminal land thoroughly with solder and then drawing off the solder with the dissolved gold using the vacuum desoldering device described in paragraph 4.3.3.

4.5.2 Harness Wiring Procedure. - The assembly sequence began with board 6 and proceeded to board 1. This reverse order kept terminal lands on the board being connected free from interfering wires, since all leads approached from below. The miniature, 37-pin test connector was temporarily taped to the front of board 6; it would be permanently attached later inside the front of the housing. The connector and its 37-wire cable fit within a channel provided in the foam so that it would be flush with the top foamed surface of board 6.

Groups of wires in several standard lengths were prepared in advance to speed assembly. The insulation was removed 0.25 inch back from one end with a thermal wire stripper, to prevent nicking the strands, and the exposed lead was then tinned. Each harness wire was inserted from the component side of the board through a hole drilled in the terminal land, then cut, clinched against the land, and soldered. A loop was formed in the wire as it was dressed around the rear edge of the board. This was done for strain relief and to provide the flexibility to permit "fanning" apart the completed stack for access to the boards after assembly. After all leads had been attached to board 6, a careful inspection was made of the solder connections, since these would be obscured after the next board was mounted.

Aluminum spacers of appropriate length were inserted in the foam cavities which surround the through-bolt holes on all boards. As each new board was added to the jig, additional 0.25-inch spacers were slipped between it and the one beneath to build in a controlled amount of slack in the harness. The extra spacers were removed as each board was completed and were transferred to the next board so that the effect was not cumulative.

Board 5 was prepared in the manner described and placed on the assembly jig. Wires which interconnected it with board 6 were attached and soldered first. Each wire was color-coded at its termination on board 5 with the same identification as was applied to the opposite end of the lead. Precut and coded wires from board 5, with free ends for connection to lower-number boards, were attached and inspected

as described for board 6. Due to the complexity of the finished harness, the accuracy of the interconnections and the quality of the solder joints were verified as each board was completed. Close collaboration between inspector and assembler was essential throughout the harness wiring operation.

Interconnections with the remaining boards in the stack were carried out step by step in the manner described. Wires to the rear connector were included in the harness as it progressed and were dressed into the connector area in the rear left corner of board 6, to be attached to the connector as the last step. The Cannon connector was temporarily attached to board 6 with a bracket which positioned it conveniently for wiring and produced sufficient slack in the finished cable for proper placement within the experiment housing. Each connector termination was sleeved with Raychem heat-shrinkable tubing from the base of the terminal solder cup to 0.1 inch above the end of the lead insulation. These sleeves isolated connections from the stresses due to the flexing of wires during mechanical assembly and provided insulation between the closely spaced terminal solder cups.

A view of the completed harness is shown in Figure 34. The harness was dressed and tied to fit freely within the 0.25-inch gap between the ends of the boards and the inside of the housing back plate.

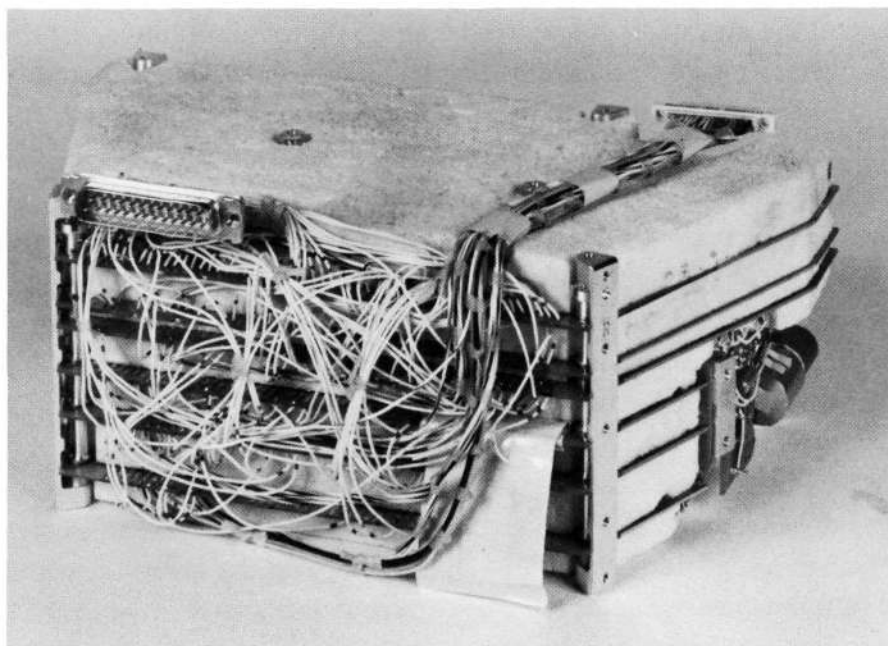


Figure 34. Electronic Stack Harness Wiring

Before installing the detector mount, which was the final operation in the electronic assembly, the stack of boards was removed from the jig and assembled with its supporting hardware. Two inboard studs were inserted through all the boards and the aluminum spacers which had been installed as each board was placed on the stack. Threaded hex bushings on the ends of the studs were tightened to hold the stack rigid for the balance of the assembly. Next, the elongated support brackets were put into place one by one. Aluminum spacers were first placed in the pockets provided for them in the foam at the edge of each board. A long bolt was then passed through the bottom end of the bracket, up through the stack, and into a washer and castellated nut where it emerged on board 6. The bolt was run through the nut and into the threaded end of the bracket until firmly in place. Compression of the stack was accomplished by tightening the castellated nuts with a special wrench.

4.5.3 Detector Mount Integration. The detector socket, installed in the back of the mount, was wired, and three bundles of leads were brought out through holes in the back cover plate. A miniature, glass-bead-type thermistor for monitoring detector temperature was epoxied into a hole drilled in the upper right corner of the back-plate mounting flange. The leads from this and the rotary solenoid installed on the side of the mount were connected to terminal studs on a small epoxy-board card behind the solenoid. Housing ground and signal ground were ac-coupled through large capacitors mounted on this card. The card terminals were interconnected with the stack by wires to a row of studs on the edge of board 4 directly above the mount.

The detector mount was prepared for integration by attaching a modified bracket to the front edge of its right side. It was then maneuvered into the front left corner of the stack in a cutout formed by successive notches in boards 1 through 3. Slots in the back cover plate of the mount engaged the outer rear corners of the notches as it was brought into position. Through-bolts inserted in the bracket and into tabs at the rear and front left corners of the mount secured it to the stack. Wires from the detector socket were connected to terminal studs on motherboard 1. The studs were arranged near their point of exit from the back cover to keep lead length to the sensitive amplifier inputs as short as possible.

4.6 Final Assembly

The housing-frame members were mounted on the stack in sequence. First, the front was attached with screws into the brackets and detector mount. Next, the sides were added, held by screws into anchor nuts on the front flanges. The back

plate was fitted into place and secured with screws which passed through its flanges, the side members, and then into threaded holes in the rear stack brackets. Two screws through the left side held the rear of the detector mount. Before any of the screws mentioned were tightened, the partially assembled experiment was installed in the assembly jig to assure trueness of the housing. The 37-pin test connector was screwed to a bracket riveted inside the front plate so that the connector body would be recessed within the housing. The main connector protruded from the rear plate, as specified, and was held by screws into captive nuts on its flanges so that the back of the housing could be removed after harness encapsulation.

The covers were held by a number of small screws in anchor nuts suitably placed around the periphery of the frame. In addition, the top surface of each cover was screwed down in two places to reduce diaphragming during vibration. The outer ends of the threaded spacers on the stud and detector through-bolt were used for this purpose.

After mechanical assembly and inspection, the experiment was electrically tested to verify correct interconnection. This was followed by high- and low-temperature tests to reveal any defective solder joints. After acceptance, the package was made ready for encapsulation of the harness wiring with silicone rubber foam (Silastic RTV S-5370, 10 pounds per cubic foot density). This flexible, sponge-like material fills voids and surrounds objects but does not adhere to smooth surfaces; it is easy to remove for repairs and can be readily patched. The initial cure takes only a few minutes at room temperature. With these ideal properties, the housing served as its own mold and no release agent was needed. The top and bottom covers were removed and the experiment, in its housing frame, was mounted on the assembly jig with the top plate off. Catalyzed foam resin was injected with a long-nozzle syringe into the middle of the harness in several places inside the back of the housing to assure uniform filling. Resin was also poured onto the test connector and cable on board 6 and distributed over the remainder of the polyurethane foam surface. The top jig plate was clamped in place to cover the open housing frame and provide a flat limiting surface for the expanding foam.

The latter part of the operation was repeated for board 1 to encapsulate the detector leads and fill the gap between the rigid foam and the cover. The housing members were removed to inspect the encapsulation. Figure 35 shows the typical results.

During reassembly of the housing after inspection, "Screw Lock," made by the Locktite Corporation, was applied to the threads of each screw before reinsertion.

This material forms a weak bond between the mating threads and prevents loosening during vibration.

4.7 Delivery

Each experiment package was protected against damage during shipment by a specially equipped carrying case. An 8 x 9 x 16 inch aluminum case, made by Halliburton, Inc., was outfitted with a thick, L-shaped aluminum mounting plate, supported on large rubber shock mounts secured inside the case to one side and the bottom. The experiment was attached to the plate with long bolts running through the four corners of the housing.

A temporary lucite cover was placed over the detector aperture to protect its 85 millionths of an inch thick titanium foil window from damage during handling prior to spacecraft integration.

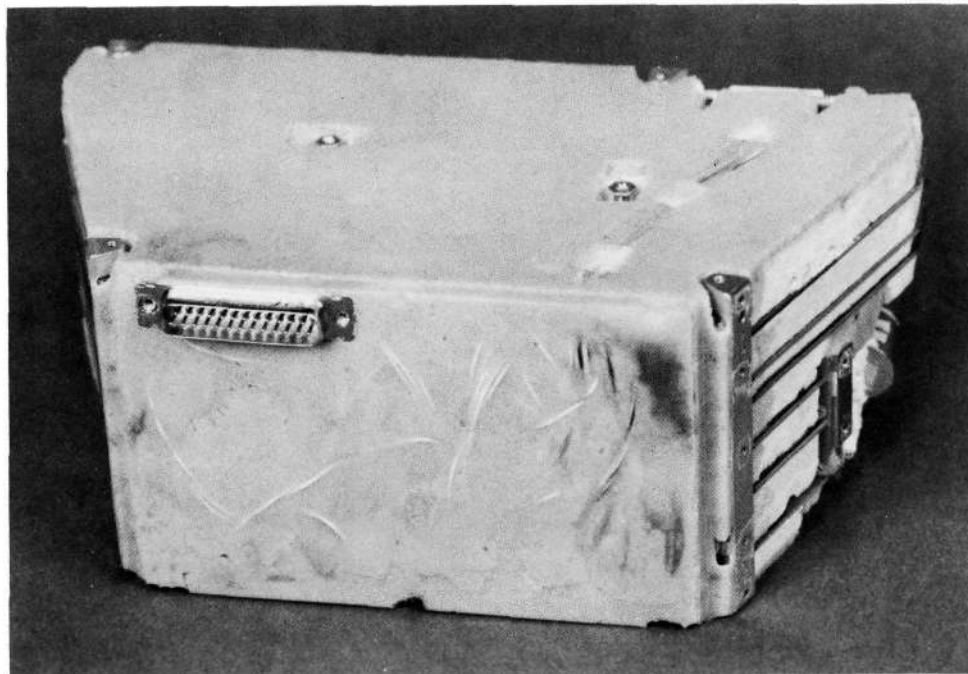


Figure 35. Encapsulated Harness

SECTION 5

HISTORY

Significant IMP-F and -G Historical Milestones

1965	December	Final weight of experiments set at approximately 3.9 pounds each.
1966	January	Contractor-owned development model ready for integration tests.
	February	First and second detector thicknesses increased to 50 microns and 100 microns, respectively. Calibration solenoid shielded with permalloy to reduce stray field. Two GSE units completed.
	March	Extensive calibration of development model with protons, deuterons, and electrons. Assembly of circuit cards begun for first flight model of IMP-F.
	April	Development model and one GSE unit delivered for integration. Completion of first flight model boards.
	May	Completion of electrical tests of first flight unit.
	June	First flight unit for IMP-F successfully passed temperature, shake, and thermal vacuum tests. This unit delivered for integration.
	July	Second IMP-F flight model successfully passed shake test and thermal vacuum test. Calibration of this unit with deuterons.
	August	Calibration of second flight model with electrons and protons. Delivery of second flight model for integration. Calibration of first flight unit with electrons and protons.
	October	Calibration of first flight unit with high-energy alpha particles at NASA/Lewis Research Center.
	November	Active area of first detectors in telescope stack increased in order to obtain higher counting rates in particle identifier modes of both IMP-F and -G.
	December	Calibration of first and second flight units of IMP-F with electrons and protons. Development of low noise preamplifier for the IMP-G experiment begun.

Preceding page blank

1967	January	Calibration of first flight unit with high-energy electrons at M.I.T. Discovery of interface problem between new IMP-F spacecraft encoder and BTL experiment.
	February	Solution of interface problem and re-qualification of modified flight units.
	March	Thermal vacuum tests of both flight units in the flight and spare spacecraft.
	April	Development work on modification of multiplier logic for the IMP-G flight unit.
	May	Successful launch of the BTL experiment on IMP-F on 24 May. Design and prototyping of the IMP-G low noise preamplifiers completed.
	August	Temperature tests on IMP-G flight unit.
	October	Calibration of the IMP-G flight unit with electrons, protons, deuterons, and alpha particles.
	November	Temperature test and qualification shake of the IMP-G unit. Calibration of this unit with protons, deuterons and alpha particles at the Bell-Rutgers facility, with electrons at M.I.T., and with alpha particles at NASA/Lewis.
	December	Delivery and integration of the flight unit.
1968	January	Thermal test of the flight unit in the spacecraft.
	May	Successful completion of all spacecraft environmental tests.
	June	IMP-G spacecraft placed in storage with solid state detectors returned to BTL for monitoring.
	November	Successful thermal vacuum test in the spacecraft.
1969	January	Kevex lithium-drifted detectors obtained for possible use in the flight experiment.
	February	Calibration of Kevex detectors.
	March	Calibration of Kevex detectors.
	April	Calibration of Kevex detectors.

May	Burn-up of IMP-F in the atmosphere on 3 May. BTL experiment operated perfectly until the bitter end. Replacement of flight lithium detectors with Kevex detectors in BTL IMP-G flight unit.
June	Successful launch of the BTL experiment on the IMP-G spacecraft on 21 June.

PRECEDING PAGE BLANK NOT FILMED

REFERENCES

1. L. J. Lanzerotti, H. P. Lie, G. L. Miller, "A Satellite Solar Cosmic Ray Spectrometer with On-Board Particle Identification," IEEE Trans. Nucl. Sci., NS-16, No. 1 (February 1969), p. 343.
2. T. C. Madden and W. M. Gibson, "Uniform and Stable dE/dx P-n Junction Particle Detectors," IEEE Trans. Nucl. Sci., NS-11, No. 3 (June 1964), p. 254.
3. I. Hayashi, H. E. Kern, J. W. Rodgers, and G. H. Wheatley, "A Vacuum Encapsulated Lithium-Drift Detector Telescope," IEEE Trans. Nucl. Sci., NS-13, No. 3 (June 1966), p. 214.
4. Final Report on Particle Detection Experiment for ATS-1, Contract No. NAS 5-9635, Bell Telephone Laboratories, Incorporated, May 1, 1969.
5. L. V. Medford, Packaging Design and Assembly of the Energetic Particles and Very Low Frequency Experiments for Project ATS, Bell Telephone Laboratories, Incorporated, Chapters 4, 5, and 6 of Reference 4.
6. F. E. Curran, I. Hayashi, L. V. Medford, and G. L. Miller, "A Modular Set of Analog Microcircuits Intended for Satellite Experiments," IEEE Trans. Nucl. Sci., NS-13, No. 1 (February 1966), p. 326.
7. R. W. Kerr, A Test Set and Procedure for Testing Tantalum Thin Film Circuit Modules, Bell Telephone Laboratories unpublished work.

Preceding page blank